Voltage Source Based Voltage-to-Time Converter

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Abstract—Voltage-to-time converter (VTC) circuits are used as the core component of single-slope analog to digital converters (ADCs). These VTC circuits have traditionally depended on the use of a constant current source as part of their implementation in order to have good linearity. An alternative approach is presented where only voltage sources and a few discrete components are needed without sacrificing linearity. This circuit can be realized in hardware using general purpose IO (GPIO) pins that are available on all microcontrollers, FPGAs, and CPLDs. This provides more flexibility than current source based VTCs that rely on specialized hardware, allowing for a full ADC to be built using GPIO pins with no specialized ADC hardware.

Keywords—voltage-to-time converter (VTC), embedded systems, analog-to-digital converters (ADC), general purpose IO (GPIO)

I. INTRODUCTION

Analog to digital converters (ADCs) are used by embedded systems in many different applications. The single-slope ADC is a simple converter that has been around for a long time [1]. At the heart of all single-slope ADCs is a voltage-to-time converter (VTC) circuit. This VTC is used to convert an arbitrary input voltage into a corresponding time with a linear relationship. A time-to-digital converter (TDC) is then used to measure the time and generate a digital value that represents the input voltage. The realization of the TDC is straightforward with a simple solution being to use a digital timer.

Existing VTC circuits are constructed using a capacitor and a constant current source [1] [2] [3]. Fig. 1 shows the schematic for a traditional VTC. Drawing a constant current out of the capacitor will cause the voltage to drop at a linear rate since \( I = C \frac{\partial V}{\partial t} \). The slope of the voltage will depend on the size of the capacitor and the magnitude of the current. By charging the capacitor up to the unknown input voltage before time 0 and then opening the switch, the time needed to discharge the capacitor has a linear relationship with the input voltage. This is how a single-slope ADC makes measurements.

Fig. 1. Current Source Based VTC Circuit

The need for a constant current source makes this VTC unattractive in many instances. When working with programmable circuits such as microcontrollers and FPGAs there are generally no constant current sources available. However, there are many controllable constant voltage sources available in the form of general purpose IO (GPIO). The GPIO allows for complete programmability and flexibility, making it an attractive option for a programmable embedded system.

Previous work has been done on using microcontrollers without hardware ADCs to measure analog values. Manufacturer application notes describe how to measure a resistance using only GPIO [4] [5]. These methods are useful for many types of measurements, but are implementations of resistance to time converters. This makes them useful for measuring certain types of sensors such as thermistors, but they cannot be used to directly measure voltages. A GPIO based VTC with a linear relationship between voltage and time is needed to enable true ADC operations within a microcontroller or FPGA with no specialized hardware.

A new VTC circuit is presented which requires only voltage sources, resistors, and a capacitor. The complete circuit is shown in Fig. 2. Special considerations are made to ensure there is a linear relation between input voltage and time. With the exception of the resistors and capacitor, all other needed components can be realized using only GPIO pins. There is calibration functionality built into the circuit allowing it to compensate for process, voltage, and temperature (PVT) effects within the GPIO pin itself. The calibration also eliminates inaccuracies due to the component tolerances of the resistors and capacitor. An analysis is presented to show how

Fig. 2. Voltage Source Based VTC Circuit
the linearity is achieved and what performance can be expected.

II. VOLTAGE-TO-TIME CONVERTER OPERATION

The time generated by the VTC circuit comes from the output of the comparator. The output signal Vo(t) will produce a step after a delay that is proportional to the voltage of Vin(t). The only difference in operation between conversions and calibrations comes from the state of SW2. When this switch is open Vin(t) feeds the RC network and is the voltage measured. When SW2 is closed Vcal feeds the RC network and the calibration voltage is measured instead.

The capacitor needs an initial condition of being discharged. This is accomplished by closing SW1 long enough to completely discharge C. The opening of SW1 marks the zero time for the VTC process. At this point the voltage of C begins charging up through the RC network. After a time proportional to the input voltage, the voltage on C will reach the value of Vref and the comparator output will transition from low to high.

With SW2 closed the input voltage to the VTC is effectively switched from Vin(t) to Vcal. In this mode the resistor Rab acts as a current limiter from the input voltage source. Since the voltage to time relationship is linear only two data points are needed to calibrate the system. Time measurements are made with two different voltages on Vcal and a simple linear interpolation is used to calibrate the system.

The key to the operation of this VTC is the combination of the large Rab resistor (Rab + Rb) connected to the input and the small Rs resistor connected to a fixed voltage, in this case Vcc. These sources in parallel across the capacitor give the equivalent circuit shown in Fig. 3.

The equivalent circuit parameters for the effective applied voltage and equivalent resistance are given in equations (1) and (3). As can be clearly seen, the equivalent circuit is a simple RC which will have an exponential time-to-voltage relationship on capacitor C. However, this exponential relationship is with respect to the equivalent applied voltage. With respect to the input voltage, the relationship is nearly linear. This is the key to the utility of this circuit.

Equation (4) gives the relationship between voltage and time when this equivalent circuit is considered in the context of the full VTC circuit. Linearization is accomplished by effectively stretching the entire time vs. voltage curve of this function. There is an asymptote that exists at the point where the applied voltage is equal to the comparator reference voltage. When time is plotted vs. the input voltage instead of the applied voltage the asymptote is shifted left and occurs at a negative voltage. This is because the 0V point of the equivalent applied voltage from (3) corresponds to a negative input voltage. This means that all positive input voltages fall farther down the curve where all that is left is the relatively linear tail of the function. The effect of this stretching and shifting can be seen in Fig. 4.

III. VTC INACCURACY MITIGATIONS

There are possible sources of measurement inaccuracy that must be analyzed. These include component tolerances, non-ideal voltage source characteristics, and the remaining non-linearity of the system.

Component tolerance inaccuracies are completely mitigated by the calibration method that is used. Since this calibration is run on the same hardware as the measurement, all these inaccuracies cancel out. The calibration process measures the timing values for two known input voltages. The effect that resistor and capacitor tolerances have on this timing will be exactly the same for both calibration and measurements, meaning the exact component values are not important. This is beneficial since it allows for lower cost, less precise components to be used without sacrificing any accuracy. The only thing important is that \( \tau_{equiv} \) should not change between the time calibration is performed and the measurement is made.

The same effect extends to the accuracies of other parts of the system, such as the timer and Vref. A very accurate timer isn’t needed as long as the repeatability of the timer is good (i.e. clock frequency is stable). The exact value of Vref is also unimportant so long as it remains constant between calibration and measurement. The calibration routine should be run...
frequently since any drift in component values between when calibration is run and when a measurement is made will result in the introduction of inaccuracies.

The circuit is shown as utilizing ideal voltage sources, but when GPIO is used to implement these voltage sources there will be some amount of series impedance as well. As long as the impedances are small when compared to the resistor values this will not have a large impact on the system performance.

While the VTC circuit described does have good linearity, it is not perfect. It is possible to bound the worst case non-linearity error. In order to determine the non-linearity error both the exact solution to the voltage vs. time and the value of a perfectly linear fit passing through the calibration points must be known. The exact solution to determine the input voltage from a time value is shown in (5).

\[
V_{in}(t) = \frac{e^{\frac{t}{\tau_{equiv}}} \cdot (R_{equiv} \cdot V_{CC} - R_S \cdot V_{ref}) - R_{equiv} \cdot V_{CC}}{(R_{equiv} - R_s) \cdot \left(e^{\frac{t}{\tau_{equiv}}} - 1\right)} \tag{5}
\]

To determine the linear fit for a function that passes through the calibration points, the times for the calibration voltages must be known. Assuming that the calibration routine uses the lower and upper bounds of voltage (e.g. VSS and VCC), the time values for the calibration points are given in (6) and (7). The linear fit using these data points in given in (8). This is a reasonable assumption for the calibration voltages. If a GPIO is used as the Vcal source then it will only have the ability to drive to a low level (VSS) and a high level (VCC) so these would have to be used as the calibration values.

\[
t_{VSS} = -\ln\left(1 - \frac{V_{ref} \cdot R_S}{V_{CC} \cdot R_{equiv}}\right) \cdot \tau_{equiv} \tag{6}
\]

\[
t_{VCC} = -\ln\left(1 - \frac{V_{ref}}{V_{CC}}\right) \cdot \tau_{equiv} \tag{7}
\]

\[
V_{in}(t) = V_{CC} \frac{t_{VSS} - t}{t_{VCC} - t_{VSS}} \cdot (t_{VSS} - t) \tag{8}
\]

Taken together, (5) and (8) can be used to determine the worst-case non-linearity error. This occurs at the maximum of the difference between (5) and (8). Taking the derivative of this difference and solving for the zero point gives the equation that specifies the time of the worst case error as shown in (9).

The equation given in (9) allows for the exact worst case error to be found but is also very cumbersome. If the circuit values that are chosen really are roughly linear, then the maximum error will fall approximately half way between the times for VSS and VCC. This time can be used together with (5) and (8) to quickly approximate the worst case non-linearity error.

While the calibration routine has the benefit of eliminating many inaccuracies in the system, it also introduces one. Rb1 acts as a current limiter during calibration and is not included in the equivalent circuit from Fig. 4. If the large resistor Rb is considered as a single value, then the value is Rb2 for calibration and (Rb1+Rb2) for measurements. If Rb2 >> Rb1 then Rb2 = (Rb1+Rb2) and the calibration results will be accurate. Increasing the size of Rb2 improves the linearity of the system, so compensating for this effect has additional benefits beyond improving calibration accuracy.

IV. VTC USE IN SINGLE-SLOPE ADC

A practical use of this VTC circuit is as part of a single-slope like ADC. This can be implemented using GPIO and a few discrete components as shown in Fig. 5. A single GPIO pin is used to implement the Vref source, comparator, and SW1. A second GPIO pin fulfills the functions of Vcal and SW2. The GPIO pins act as voltage sources when configured as outputs, which performs the function of “closing” the switches. The pins act as comparators with high input impedance when configured as inputs. The high impedance effectively “opens” the switch in this state. The GPIO threshold voltage is equivalent to Vref. The resistors and capacitors are implemented with discrete components. A timer peripheral is used to perform the TDC.

The system performs calibration by setting the CAL pin to an output and setting the value low. A measurement is made and the time is recorded. The CAL output is then set high and a second measurement is made. A linear interpolation is used to map all future time values between these two points.

The resolution of the ADC is ultimately determined by how long it takes the RC circuit to charge versus the timer frequency. Since the relationship between time and voltage is

![VCC](image-url)
linear, the number of different voltage levels that can be distinguished by the ADC is equal to the difference between the timers with an input of VSS and an input of VCC. Expressing this in terms of bits of resolution based on the timer frequency is done according to (10).

\[ \text{Resolution} = \log_2 \left( \left| f \cdot t_{\text{VSS}} \right| - \left| f \cdot t_{\text{VCC}} \right| \right) \] (10)

The hardware imposed maximum sampling speed of the ADC is determined by two factors. The first part is the time needed to establish the initial condition on the capacitor. This time is dependent on the size of the capacitor and the output impedance of the GPIO pin. The second part is determined by the amount of time it will take for the capacitor to charge back up to the threshold voltage. This time must be considered in the worst case, which would be when the threshold voltage is the highest and the applied input voltage is the lowest. This is shown in (11), where the time to set the initial condition is assumed to be 5 time constants of the capacitor and GPIO output impedance.

\[ \text{ADC Frequency} = \frac{1}{5 \cdot R_c \cdot C \cdot \ln \left( \frac{V_{\text{ref}}}{V_{\text{applied}}} \right) \cdot \tau_{\text{equiv}}} \] (11)

As previously mentioned, the accuracy of this ADC is very good. This is due to the calibration process which can compensate for component tolerances, timer inaccuracies, and PVT drift in component values. Using the ADC resolution from (10) along with the maximum error from (9) allows for easy analysis of the non-linearity effects. As long as the non-linearity error is less than the resolution of the ADC, then these effects can be ignored and the system will perform as if the VTC was perfectly linear.

V. EXPERIMENTAL RESULTS

An example system was constructed using this VTC circuit with GPIO pins on Microchip PIC16F1513 microcontroller. The system was operated at 5V with TTL thresholds. The frequency of the counter used for the TDC was 4 MHz. The expected performance was 6 bits of resolution at a 2.2 kHz sampling rate. Actual data captured using this ADC is shown in Fig. 6.

The actual resolution of the system was measured at 6.4 bits due to the threshold voltage actually falling slightly above the worst case. The sampling rate achieved was 2 kHz, which is slightly lower than expected due to some software overhead required between conversions.

VI. ADDITIONAL CONSIDERATIONS

This paper was written from the standpoint of charging the RC network while making a time measurement. It is also possible to conceptually flip this entire process upside down and discharge the RC network by setting the initial condition of the capacitor to VCC and tying Rs to VSS. This can be advantageous in some circumstances. For example, in a 5V system with TTL inputs the worst case resolution occurs when the threshold voltage is 0.8V. If discharging is used instead the worst case resolution threshold voltage is effectively 3V (discharging from 5V down to 2V). Larger voltage changes equate to longer times and higher measurement resolutions at the cost of slower speeds. If the voltage driving Rs is controlled by another GPIO pin, then charging or discharging mode could be selected on the fly. This allows for dynamically switching between a higher resolution measurement and a faster speed measurement. This simple change allowing for dynamic performance adjustment could be useful in many situations.

While this system was considered for cases where the input voltage is between VSS and VCC this is not a strict requirement for the operation of the VTC circuit. With minor modifications the circuit is actually capable of making measurements for voltages that go well beyond the rails. This could be exploited to create a simple GPIO based ADC with an ability that is lacking in most hardware ADCs, namely the ability to directly measure negative voltages.

VII. CONCLUSION

A VTC realized without using a constant current source was presented. The use of only voltage sources and discrete components allows for implementations based on any device with GPIO. It was shown that this VTC can be used as part of an ADC implementation. This could be extended to any parts with GPIO such as high performance, high pin count FPGAs. In that case, this could provide a method for performing hundreds of parallel analog to digital conversions at the same time with low resource utilization and a relatively simple implementation.

REFERENCES