1. A computer system uses 4-megabit memory chips and a 64-bit data bus. Draw a diagram and show the minimum number of memory chips we can use for each of the following chip configurations. What is the resulting minimum amount of memory (in bytes) we can use in a system for each chip configuration?

   a.  4 Meg x 1
   b.  1 Meg x 4
   c.  256K x 16

We need 64 data lines in parallel for each of the configurations. So, we assemble the minimum number of chips that will give 64 data lines out.

   a.  64 chips x 4 megabits per chip = 256 megabits = 32 megabytes minimum memory.

   1  2  3  4  63  64
   4 M x 1 4 M x 1 4 M x 1 4 M x 1

   b.  16 chips x 4 megabits per chip = 64 megabits = 8 megabytes minimum memory.

   1  2  3  4  15  16
   1 M x 4 1 M x 4 1 M x 4 1 M x 4

   c.  4 chips x 4 megabits per chip = 16 megabits = 2 megabytes minimum memory.

   1  2  3  4
   256K x 16 256K x 16 256K x 16 256K x 16
2. The 4-megabit memory chips are placed onto modules (SIMMs or DIMMs) of 8 megabytes each. Select an appropriate chip organization to use for each of the following module configurations, draw a diagram and show the minimum number of modules we can use for each. What is the resulting minimum amount of memory (in bytes) we can use with the 64-bit data bus system for each module configuration?

a. 72 pin SIMM (32 bit data lines).

b. DIMM (64 bit data lines).

We need 8-megabyte modules made up of 4-megabit chips, so we need a total of 16 chips per module. The system bus needs 64 data lines in parallel for each of the configurations. So, we assemble the minimum number of SIMMs or DIMMs that will give us 64 data lines out.

a. The SIMMs have 32 data lines out, so we can’t use the 4 meg x 1 organization; it would give us only 16 data lines out. We can use either the 1 meg x 4 or the 512k x 16 chips. It is normally cheaper to use the memory chip with the fewer number of larger arrays, so we choose the 1 meg x 4 organization. Each SIMM has 32 data lines, but we need 64 data lines for the system bus, so we need a minimum of two SIMMs. 2 SIMMs x 8 megabytes each = 16 megabytes minimum memory.

b. The DIMMs have 64 data lines out, so we can again use either the 1 meg x 4 or the 512k x 16 chips. We choose the 1 meg x 4 organization. Each DIMM has 64 data lines, so we need only one DIMM. 1 DIMM x 8 megabytes = 8 megabytes minimum memory.
3. Assume we have a fast processor such that the memory system is 100% utilized. The processor accesses memory in a totally random fashion. Using the memory specifications given in class, what is the effective average access time (per word) the processor would see for the following types of memory?

   a. 50 ns FPM DRAM
   b. 50 ns EDO DRAM
   c. 10 ns SDRAM (100 MHz clock)
   d. 4 ns SRAM

The memory access rate is limited by the RAS cycle time for each of the DRAM memories. For the SRAM memory, it depends on whether or not we can anticipate where we will read the next memory address before we get data back from the current address.

   a. \( t_{RC} \) Cycle Time = 95 ns for the 50 ns FPM DRAM. Therefore, average access time for the FPM DRAM is 95 ns.

   b. \( t_{RC} \) Cycle Time = 84 ns for the 50 ns EDO DRAM. Therefore, average access time for the EDO DRAM is 84 ns.

   c. \( t_{RC} \) Bank Cycle Time = 8 clocks for the 10 ns SDRAM clocked at 100 MHz. Therefore, average access time for the 10 ns SDRAM is 80 ns.

   d. \( t_{CYCLE} \) Cycle Time = 10 ns for the 4 ns SRAM. Therefore, average access time for the SRAM is 10 ns IF we can always anticipate subsequent addresses. If we must wait to retrieve data from the current address before we know where we will read the next address (the likely case), the average access time is 20 ns (2 clocks).
4. Assume the same processor and memory as problem #3. The processor accesses memory in a totally random fashion, but always accesses 4 sequential words (at 4 sequential addresses) at each of the random locations. What is the average access time (per word) the processor would see for the following types of memory?

a. 50 ns FPM DRAM
b. 50 ns EDO DRAM
c. 10 ns SDRAM (100 MHz clock)
d. 4 ns SRAM

Since we are reading from 4 sequential locations each time, we don’t need to assert RAS on each access for the DRAMs. However, we still need to allow for the precharge time on each 4 accesses. Therefore, we will need 1 RAS cycle time plus three CAS cycle times for each 4 accesses.

a. \( t_{RC} \) Cycle Time = 95 ns and \( t_{PC} \) Fast Page Mode Cycle Time = 35 ns for the 50 ns FPM DRAM. Therefore, average access time = \( (95 + 3 \times 35)/4 = 50 \text{ ns} \).

b. \( t_{RC} \) Cycle Time = 84 ns and \( t_{HPC} \) EDO (Hyper Page) Mode Cycle Time = 20 ns for the 50 ns EDO DRAM. Therefore, average access time = \( (84 + 3 \times 20)/4 = 36 \text{ ns} \).

c. \( t_{RC} \) Bank Cycle Time = 8 clocks and we can read subsequent data out in 1 clock increments for the SDRAM. Therefore, average access time = \( (80 + 3 \times 10)/4 = 27.5 \text{ ns} \).

d. \( t_{CYCLE} \) Cycle Time is 10 ns for the 4 ns SRAM. If we can anticipate subsequent random locations (every 4\(^{th}\) read which is random), the average access time is \( (10 + 3 \times 10)/4 = 10 \text{ ns} \). If we can’t anticipate random reads before we complete the current access, we have to wait 2 clocks to get the first word. Therefore, the average access time is \( (20 + 3 \times 10)/4 = 12.5 \text{ ns} \).
5. Assume a memory system using a 64-bit word length and 4 interleaved memory banks with a total of 16 megabytes of memory. Show which bits of the memory address are used to address byte, bank and, word within a bank.