
1. A computer system uses 4-megabit memory chips and a 64-bit data bus. Draw a diagram and show the minimum number of memory chips we can use for each of the following chip configurations. What is the resulting minimum amount of memory (in bytes) we can use in a system for each chip configuration?
   a. 4 Meg x 1
   b. 1 Meg x 4
   c. 256K x 16

2. The 4-megabit memory chips are placed onto modules (SIMMs or DIMMs) of 8 megabytes each. Select an appropriate chip organization to use for each of the following module configurations, draw a diagram and show the minimum number of modules we can use for each. What is the resulting minimum amount of memory (in bytes) we can use with the 64-bit data bus system for each module configuration?
   a. 72 pin SIMM (32 bit data lines).
   b. DIMM (64 bit data lines).

3. Assume we have a fast processor such that the memory system is 100% utilized. The processor accesses memory in a totally random fashion. Using the memory specifications given in class, what is the effective average access time (per word) the processor would see for the following types of memory?
   a. 50 ns FPM DRAM
   b. 50 ns EDO DRAM
   c. 10 ns SDRAM (100 MHz clock)
   d. 4 ns SRAM

4. Assume the same processor and memory as problem #3. The processor accesses memory in a totally random fashion, but always accesses 4 sequential words (at 4 sequential addresses) at each of the random locations. What is the average access time (per word) the processor would see for the following types of memory?
   a. 50 ns FPM DRAM
   b. 50 ns EDO DRAM
   c. 10 ns SDRAM (100 MHz clock)
   d. 4 ns SRAM

5. Assume a memory system using a 64-bit word length and 4 interleaved memory banks with a total of 16 megabytes of memory. Show which bits of the memory address are used to address byte, bank and, word within a bank.