CSC506 Vector Processor Homework – due Friday, June 11, 1999

Q1. A low-order interleaved memory has 32 memory modules that are addressed by word and numbered 0, 1, …, 31. If the processor generates a word address in the Memory Address Register (MAR) of A45C23B, which memory module will be accessed?

Q2. A company builds a vector computer with eight parallel processors at a clock rate of 400 MHz. If one of the vector instructions generates a scalar by multiplying two vectors and summing the products, what FLOPS rate can the vendor claim?

Q3. What is the memory bandwidth (in words/sec) required to support ***each processor*** in question 2? (Note that the maximum will occur on V ← V x V type vector instructions.)

Q4. Use the vector computer and vector instruction described in question 2. The floating point ***add*** pipeline is 4 stages and the floating point ***multiply*** pipeline is 10 stages. What is the effective speedup for vectors of length 8? What is the effective speedup for vectors of length 1000?

Q5. A vector load instruction is used to load a vector of length 100 from 8 interleaved memory modules into a vector register of a processor. The memory is organized like the diagram on page 14 of the class notes and each memory unit is built up of SDRAM clocked at 100 MHz needing 6 clocks for RAS access time and 8 clocks cycle time. If the data bus runs at 800 MHz and transfers one word at a time from the memory system to vector register:

a. how long does it take for a vector with unit stride to load?
b. how long does it take for a vector with a stride of 2 to load?
c. how long does it take for a vector with a stride of 8 to load?