CSC506 Homework due Friday, 6/18/99 - Switch Questions

1. We have a three-stage Omega (Shuffle-exchange) network to connect eight processors numbered P0, P1, … P7 to eight independent memory modules numbered M0, M1, . . . M7.
   a) Draw the network.
   b) Show (highlight) the following connections through the network:
      P0 → M2, P4 → M4, P6 → M3.
   c) Can these accesses be performed concurrently or do they conflict?
   d) Add a processor-to-memory access that is blocked (conflicts) by one of the accesses used in part b).
   e) Add a processor-to-memory access that is not blocked by one of the accesses used in part b).

2. The Omega network in question 1 needs to provide a path of 128 data lines and 32 address lines:
   a) How many individual switches are required to implement the network?

   b) If we implemented a full crossbar switch in place of the Omega network, how many individual switches would be required?

   c) What would be the corresponding number of switches in both cases for a 16 processor, 16 memory system?