Macromodels of Digital Integrated Circuits for High-Speed Digital Circuit Simulation

by

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Abstract

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A technique for developing macromodels of digital integrated circuits using non-linear table-based methods is presented. The technique is based on a behavioral modeling approach using one-port and two-port macromodels which describe the input and output characteristics and the internal characteristics of the device. The one-port and two-port macromodels are developed from DC and scattering parameter measurements of the device.

Based on the one-port and two-port macromodeling techniques, a NAND gate macromodel is developed. To determine the one-port macromodel components, the scattering parameters of the macromodel are fitted to the scattering parameters of the actual device through optimization. The one-port macromodel components are estimated from scattering parameter measurements using a FORTRAN routine. Scattering parameter results are presented for the NAND gate macromodel. In addition, the DC and transient analysis results of the NAND macromodel are presented. The DC results include the I-V curves and the voltage transfer characteristics of the device. The transient analysis results include a simple NAND gate circuit and a NAND gate driver-receiver, commonly used in digital circuit simulation. The macromodel provides an accurate time-domain model with a factor of five to ten computational speed increase over that of the transistor-level model. Good agreement was obtained.
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List of Symbols and Abbreviations

$\omega$ — angular frequency

ACL — advanced complementary metal-oxide logic

ALSTTL — advanced low-power schottky transistor-transistor logic

ASTTL — advanced schottky transistor-transistor logic

CAD — computer-aided design

CMOS — complementary metal-oxide semiconductor

CPU — central processing unit

DC — direct current

ECL — emitter coupled logic

GaAs — gallium arsenide

IC — integrated circuit

I-V — current-voltage

LSI — large scale integration

LSTTL — low-power schottky transistor-transistor logic

RC — resistor-capacitor

TTL — transistor-transistor logic

VCCS — voltage-controlled current source

VCVS — voltage-controlled voltage source

$Y_c$ — characteristic admittance

$Z_c$ — characteristic impedance
Chapter 1

Introduction

1.1 Motivation

As clock rates and edge rates in digital systems increase, the need for accurate simulation of the digital system becomes crucial for locating high-frequency problems. These problems are manifested as transmission line effects and crosstalk. The increased clock rates and edge rates enhance transmission line effects and crosstalk, which can degrade system performance. Therefore, to improve system performance, the high-frequency problems must be located and eliminated from the digital system. The most cost-effective way to enhance system performance is to remove potential high-frequency problems in the digital system at the design stage. High-speed digital circuit simulation can detect any problem areas in the design, thus eliminating potential high-frequency problems and enhancing system performance and operation.

High-speed digital circuit simulation involves either the timing analysis of the digital system or the analog analysis of the system's signals. Although the digital system's overall function is digital, internally, the signals are strictly analog. Consequently, the simulation of high-speed frequency effects, such as transmission line effects and crosstalk, is best performed using an analog circuit simulator. However, there is a price to pay for using an analog circuit simulator. Analog simulation of a digital system is slow and CPU expensive. All components in the system must be correctly modeled for accurate simulation results. Digital integrated circuits and
transmission lines are the primary concern. The physical models for digital integrated
circuits consist of transistor-level models, and the physical models for transmission
lines consist of distributed lumped-element models. These models are complex, and
thus significantly slow down the simulation and cause convergence problems.

Traditionally, digital integrated circuits have been modeled by either transistor-
level models or by simple lumped element models. Both approaches have their advan-
tages and disadvantages. Transistor-level models are accurate, however, they require
large amounts of memory, are computationally slow, and often have convergence
problems due to the large number of components. Simplified lumped element models
are computationally fast and use small amounts of memory, however, they are often
inaccurate. By utilizing the advantages of both transistor-level models and lumped
element models, table-based macromodels provide an alternative to modeling digital
integrated circuits.

The digital integrated circuit macromodel is based on an analog behavioral model
approach, shown in Figure 1.1.1. The macromodel is divided into three stages which
represent the internal and external characteristics of the device. Each stage is con-
structed based on a black-box representation of the device, shown in Figure 1.1.2.
First, the input stage models the input impedance $Z_i$ of the device. The input impedance is a nonlinear function of the input voltage $V_i$ and the input current $I_i$. Second, the delay stage models the propagation delay of the device. The delay stage also controls the logic operation of the device by transferring the voltage at the input stage to the output stage. Third, the output stage models the output impedance $Z_o$ and the logic operation of the device. The output impedance is a nonlinear function of the output voltage $V_o$ and the output current $I_o$, and ideal switches ensure the correct impedance as a function of the device state. In addition, the output stage ensures the correct sourcing and sinking of output current as a function of the output load.

The objective of the macromodeling technique is to provide a time-domain model of digital integrated circuits which is accurate to within 10 to 20 percent of the actual device and offers a computational speed increase of 5 to 10 times that of the device's transistor-level model. As an example, the macromodeling technique is applied to a TTL NAND gate. The technique can also be expanded to work for other devices and logic families. The macromodels can be implemented in an analog circuit simulator.
for use in high-speed digital circuit simulation.

Macromodeling of digital integrated circuits has been an increasingly popular research area in the last decade. Early macromodeling work in the mid-1970s was limited to digital integrated circuits such as NAND gates and flip-flops. In the last few years, macromodels of more complex integrated circuits, such as operational amplifiers, have been developed. Macromodeling research and development will increase in the next several years as designs become more complex and digital system clock rates continue to increase.

The purpose of this thesis is to present an approach for macromodeling digital integrated circuits based on table-based and behavioral modeling techniques. As an example, a NAND gate macromodel is developed and implemented in SPICE for use in high-speed digital circuit simulation.

1.2 Thesis Overview

This thesis provides the background theory and methodology for developing and implementing macromodels of digital integrated circuits for high-speed digital circuit simulation. The thesis is divided into four primary sections. First, a review of previous work and macromodeling theory is presented. Second, the development of one-port and two-port macromodels are discussed. Third, a NAND macromodel is implemented in SPICE, an analog circuit simulator. Lastly, results are presented for the NAND macromodel. The thesis consists of seven chapters and three appendices.

Chapter 2 consists of a literature review and an introduction to one-port and two-
port macromodels. The literature review is a summary of macromodel types and a review of previous macromodeling work. Three examples of NAND gate macromodels are presented. The advantages and disadvantages of each macromodel example are discussed. In addition, the introduction to one-port and two-port macromodels discuss the characteristics of the one-port and two-port models.

Chapter 3 presents the development of one-port macromodels. The input and output characteristics of TTL devices are presented. An example of a NAND gate macromodel is discussed. Techniques for determining the input and output characteristics of the NAND gate are presented. These techniques include I-V curve measurements and scattering parameter measurements. The I-V curve measurements are used for determining the nonlinear input and nonlinear output resistance of the device. The scattering parameter measurements are used for determining the input and output lead resistance, lead inductance, and nonlinear capacitance of the device. Scattering parameter and transmission line background is presented. The calculation of the macromodel components from scattering parameter measurements is presented. In addition, the equations describing the macromodel and the scattering parameter measurements are presented. Lastly, scattering parameter optimization using a computer-aided design package is discussed.

Chapter 4 presents the development of two-port macromodels. The internal characteristics of the device, which include current drive capability, logic operation, propagation delay, and ground noise, are discussed.

Chapter 5 presents the development and implementation of a NAND gate macro-
model. The SPICE macromodel of a TTL NAND gate is presented. The macromodel's input stage, delay stage, and output stage are discussed. In addition, the macromodel's approach to ground noise modeling is discussed. Problems and limitations of the model, which include the single-input stage, linear resistors, linear capacitors, and convergence problems, are discussed.

Chapter 6 presents the results and discussion of the NAND gate macromodel. DC analysis results, including the input I-V curve, the output I-V curve, and the voltage transfer characteristics, are presented. Transient analysis results are presented. The transient analysis results include simulations on two different NAND gate circuits: a simple NAND gate circuit terminated in a resistive and capacitive load, and a NAND gate driver-receiver circuit. The results consist of comparisons between circuit simulations made with both the macromodel and the transistor-level model.

Chapter 7 is the conclusion and summary of work accomplished. Suggestions for future work are also discussed.

The thesis contains three appendices. Appendix A presents background work on ground noise in digital systems. Appendix B is a discussion of nonlinear devices and their implementation in SPICE. Appendix C contains the SPICE circuit file of the NAND gate macromodel and a user's guide.

1.3 Original Contributions

Original contributions reported in the thesis include:
1) a technique for extracting impedance information from DC I-V curve measurements and frequency-domain scattering parameter measurements,

2) a technique for providing simulated I-V curve data for a device using SPICE,

3) development of a macromodeling technique based on table-based and behavioral modeling, and

4) a SPICE compatible TTL NAND gate macromodel.
Chapter 2

Review of Macromodeling Theory

2.1 Introduction

This chapter presents a literature review of past macromodeling theory and an introduction to one-port and two-port macromodels. The literature review consists of a description of macromodel types and three NAND macromodel examples from previous papers. The introduction to one-port and two-port macromodels consists of defining a macromodeling approach based on previous macromodeling work.

The literature review presents previous macromodeling work of the 1970s and the early 1980s. First, a description of six macromodeling types are presented. The macromodeling types are based on two approaches: a mathematical model utilizing a nonlinear system of equations, and a circuit behavioral model, which describes the input and output characteristics using a lumped-element model. Second, three NAND gate examples are discussed. Developed during the 1970s and early 1980s, the NAND gate macromodels are the earliest attempts at macromodeling work. The macromodels are crude and do not provide the accuracy needed under all operating conditions. If increased accuracy is desired, the macromodels can be enhanced using a macromodeling technique consisting of one-port and two-port macromodels.

The one-port and two-port macromodeling technique presents an improvement over previous macromodeling techniques. The technique consists of developing nonlinear lumped-element models based on systematic measurements of the device. The
technique consists of a two step process. First, the one-port macromodels are developed. The one-port macromodels describe the external characteristics of the device. Second, the two-port macromodel is developed based on the one-port macromodels and the internal characteristics of the device. The two-port macromodel describes the complete device, including the internal and external characteristics.

2.2 Literature Review

Traditionally, macromodels and macromodeling techniques were developed out of a need for fast and accurate models of large-scale integrated circuits. Most of the previous macromodeling theory was done in the 1970s and early 1980s, as computer-aided design of digital circuits became more pronounced. Presently, the demand for macromodels of integrated circuits has increased, spawned by the need for CAD simulation of high-speed digital systems.

The choice for using macromodels is twofold. First, the macromodels provide an accurate time-domain model of an integrated circuit that is within 10 to 20 percent of the original device. Second, the macromodel offers a computational speed increase of 5 to 10 times that of a transistor-level model of the device. This speed increase is essential for simulating large digital systems containing many integrated circuits.

In the past, many macromodeling techniques existed for modeling digital integrated circuits, specifically large-scale integrated circuits (LSI). The most popular techniques included time-domain approaches, mathematical approaches, and lumped-element circuit behavioral approaches.
The time-domain approach involved using a time-domain model based on a latent or a sensitivity approach for analyzing a nonlinear system. Hsieh and Rabbat produced two papers describing a macromodeling and latent technique for modeling LSI circuits. First, in 1977, a macromodeling and latent technique for computer-aided design of large networks was presented [1]. Second, in 1979, the technique was further expanded into a multilevel Newton algorithm for the analysis of nonlinear circuits in the time-domain [2]. In 1982, Lelarasmee, Ruehli, and Sangiovanni-Vincentelli developed a waveform relaxation method for modeling LSI circuits in the time-domain [3]. These approaches were fairly accurate, but did not provide the speed increase needed for simulating large digital systems and were incompatible with analog circuit simulators such as SPICE.

The mathematical approach consisted of representing the device by a system of equations. A system of differential and algebraic equations described the nonlinear system or device. In 1983, Schilling and Rahmani developed a representation theorem for nonlinear systems with piecewise-constant inputs [4]. The physical system is modeled by nonlinear and algebraic equations, which is a function of the state of the system, the input, and the output of the system. For each piecewise-constant input, under certain restrictions, a corresponding output is determined. The mathematical approach produced tedious equations that were often difficult to solve for complex systems, and often the models were limited by assumptions placed on the system or the input waveform.

Lumped-element circuit behavioral macromodels consisted of a simplified lumped-
element model which described the original system or device. The components of the model could be linear or nonlinear. In 1973, Greenbaum developed a lumped-element macromodel for a flip-flop [6] and a NAND gate [5]. In 1978, Glesner expanded on the lumped-element macromodel approach, providing a more accurate model of the NAND gate [7]. Also, in 1980, Bakhov developed a NAND gate macromodel, using a technique similar to Greenbaum’s and Glesner’s [8]. The lumped-element macromodels provided a significant computational speed increase over other macromodel techniques, however, the model lacked the accuracy of the actual device.

This section presents several macromodel types and three examples of a NAND gate macromodel. The macromodels are previous attempts at developing simplified lumped-element models of a NAND gate device.

2.2.1 Macromodel Types

Macromodeling is a technique for reducing a complex system or device to a simplified model of the system or device. The macromodel describes the internal and external characteristics of the complex system or device. The macromodel consists of mathematical equations or an equivalent lumped-element model which describe the static and dynamic characteristics to the same degree of accuracy as the original system or device [4].

Hsieh and Rabbat define five common types of macromodels [9]:

1) Circuit Reduction Macromodel

The circuit reduction macromodel consists of a circuit which is simpler than the
original circuit. This macromodel is obtained in two ways:

i) replacing the original circuit components one at a time with short or open circuits until the input and output characteristics of the original circuit deviates more than the error limits, or

ii) using the sensitivity approach. The dominant components for the original circuit are found using sensitivities of the original circuit. These dominant components are used to develop the macromodel. The number of components used depends on the accuracy required.

2) Circuit Behavior Macromodel

The circuit behavior macromodel describes the external characteristics of the original circuit. The macromodel is characterized by input and output impedance, delays, and terminal circuit properties. Internal elements of the macromodel may not resemble the original circuit or may have little physical significance.

3) Table Behavior Macromodel

The table behavior macromodel uses a numerical table to represent the original circuit. A table stores the input and output characteristics of the device for various inputs and loading conditions. The table entries are obtained from manufacturer's data on the device or from experimental measurements. In a table look-up format, the macromodel is easily automated for computer simulation.

4) Mathematical Macromodel

The mathematical macromodel consists of using various mathematical techniques
to represent the circuit components. For example, differential equations or polynomials may describe a controlled source or a nonlinear element. A probability density function may describe the input and output propagation delays at various voltage levels. Using the mathematical technique to develop macromodels requires intimate knowledge of the system's behavior. Furthermore, the equations describing the system or device are often complex and tedious due to the large number of components.

5) Symbolic Macromodel

The symbolic macromodel is obtained by symbolic formulation of the original circuit subnetwork. Examples of symbolic elimination are matrix formulation and ordering and Gaussian elimination. An example of symbolic macromodel is the function oriented symbolic macromodel (FOSM).

6) Combination of Macromodel Types

Often, a macromodel may consist of several different model types. For example, a digital integrated circuit can be described by multiple macromodel types:

- a circuit behavior macromodel and a table behavior macromodel to describe the input and output characteristics of the device, and

- a mathematical or symbolic macromodel to describe more complex components, such as controlled sources and nonlinear elements, and to describe the internal characteristics, such as the propagation delays.

Keeping the macromodel as general and simple as possible results in a savings in computer storage and computational time.
In summary, the macromodel approaches can be grouped into circuit techniques and mathematical techniques [10]. The macromodels are constructed based on network reduction, terminal characteristics, experimental data, and mathematical functional descriptions. Time-domain methods of analysis include nonlinear time-domain methods, latent nonlinear time-domain methods, and piecewise linear time-domain methods.

2.2.2 TTL NAND Gate Macromodel Examples

This section presents three examples of TTL NAND gate macromodels. The macromodels were developed by Greenbaum, Glesner, and Bakhov in 1973, 1978, and 1980, respectively. The NAND gates are dual-input, positive logic devices. The macromodels model the input, output, and internal characteristics of the gate.

Greenbaum Model [5]

The Greenbaum model is shown in Figure 2.2.1. The model consists of three stages:

1) Input stage
   - input characteristics

2) Middle stage
   - logic state
   - propagation delay

3) Output stage
   - transfer characteristics
   - output characteristics
Figure 2.2.1: Greenbaum's NAND gate macromodel

**Input Stage:**

Current sources $J_A$ and $J_B$ model the input characteristics of the gate. The current sources are zero-valued, thus providing an infinite input impedance. This provides a good first-order approximation, since the input impedance of a NAND gate is in the kΩ range. If increased accuracy is needed, Greenbaum suggests modeling current sources $J_A$ and $J_B$ in diode equation format or as tables of current as a function of applied voltage.

**Middle Stage:**

Dependent voltage source $E_1$ establishes the logic state of the gate. If either of the input signals is less than or equal to 0.8 V (maximum logic 0 input voltage), then $E_1$ is set to 3.1 V (maximum logic 1 output voltage). If both input signals are equal to or greater than 1.9 V (minimum logic 1 input voltage), then $E_1$ is set to 0.3 V (maximum logic 0 output). If neither of these conditions exist, for example, when the input is in a transition state, then $E_1$ is set to 3.1 V minus the absolute value of the smaller of the two input signals. A computer routine calculates the value of $E_1$. 
The resistor $R_1$ and the capacitor $C_1$ model the propagation delays of the gate. A routine determines the value of capacitor $C_1$. $C_1$ is set at 550 pF, except when voltage $E_1$ is less than voltage $E_2$, then $C_1$ is set to 300 pF. In general, the two propagation delays, low-to-high and high-to-low transitions, are not equal. Therefore, if alternate propagation delays are needed, then $C_1$ can be adjusted accordingly.

**Output Stage:**

The voltage-controlled voltage source $E_2$ establishes the transfer characteristics of the device. $E_2$ is a function of the voltage across capacitor $C_1$, which is a function of $E_1$. Therefore, $E_1$ and $E_2$ are related, and a relationship between the input and the output signals exists.

The resistor $R_2$ models the output characteristics of the device. $R_2$ is fixed at 30 Ω. This does not model the output characteristics accurately for all input and load conditions, but it does provide a first-order approximation for the output signal level. The zero valued current source $J_o$ is a reference component which serves to monitor the output signal under various input and load conditions.

Greenbaum presents results showing agreement of the NAND gate model with the actual device.

**Glesner Model [7]**

The Glesner model is shown in Figure 2.2.2. The model consists of three stages:

1) **Input stage**
   - input characteristics
   - logic operation
2) Middle stage
   - voltage transfer characteristics
   - transition times

3) Output stage
   - propagation delay
   - output characteristics

**INPUT STAGE:**

The current sources $J_A$ and $J_B$ model the input characteristics of the device. The current sources are nonlinear and depend on their respective input voltages. Glesner users a table of values to represent each current source, which can be easily implemented in a simulation program.

The input stage also models the logic operation of the device. A logic state parameter, $PL$, performs the AND operation on the input signals, given by $PL = MIN(V_{J_A}, V_{J_B})$, where $V_{J_A}$ and $V_{J_B}$ are the node voltages at input A and input B, respectively. The AND operation is equivalent to taking the minimum of all input signals. The logic stage parameter allows expansion of the macromodel into multiple inputs by evaluating the MIN function on all input voltages.
MIDDLE STAGE:

The voltage source $E_1$ models the transfer characteristics of the device. The voltage transfer characteristics of the gate perform an inversion of the input signal. A look-up table stores the transfer characteristics of the gate, which is assigned to the source $E_1$. Thus, given an input voltage, the corresponding voltage at $E_1$ represents a NAND function.

The resistor $R_1$ and capacitor $C_1$ provide a low pass network, which simulates the transition times of the gate. The rising and falling edges of the output signal are modeled by two values of the capacitor $C_1$.

The current source $J_O$ serves as a reference component for the DC analysis and transfers the output voltage of the low pass network to the output stage.

OUTPUT STAGE:

The voltage source $E_O$ models the average propagation delay of the gate. $E_O$ is a function of $V_{J_R}$, the voltage across current source $J_R$. The variable PDT represents the average of the two propagation delay times, $t_{pLH}$ (low to high propagation delay) and $t_{pHL}$ (high to low propagation delay). A FORTRAN subroutine simulates the delay function in the time-domain. Values of $V_{J_R}$ are stored in a delay table at time $t_k$ ($t_k$ is the time point of the $k^{th}$ integration step) and read out at time $t_k + PDT$.

The resistor $R_O$, capacitor $C_L$, and current source $J_O$ model the output characteristics of the device. Glesner uses a linearized version of the output characteristics simulated using SPICE. From the output characteristics, the output resistance $R_O$ and the positive and negative output current limitations, PSP and PSN, are com-
puted. \( R_O \), PSP, and PSN are all a function of the logic stage parameter PL. The values of \( R_O(PL) \), PSP(PL), and PSN(PL) are read from the simulated linearized characteristics and stored into three tables. The current through the output resistor \( R_O \), \( I_{RO} \), controls the current generator \( J_O \). If \( I_{RO} \) exceeds the current limitations PSP or PSN, then the current source \( J_O \) increases or decreases linearly to hold the output current constant. The output capacitance of the gate, \( C_L \), is fixed at 15 pF.

Glesner uses a three-stage ring oscillator to test the transient response of the macromodel. The macromodel simulation and actual device measurements agree within five percent. In addition, Glesner uses the macromodel to study the propagation of digital signals on transmission lines. The test circuit consists of two NAND gates interconnected by a coaxial cable. To demonstrate the effects of ringing, two different characteristic impedances of the coaxial cable, 50 \( \Omega \) and 240 \( \Omega \), are used in the simulation. The results agree well with laboratory measurements.

**Bakhov Model [8]**

The Bakhov model is shown in Figure 2.2.3. The model consists of three stages:

1) Input stage
   - logic operation
   - input characteristics

2) Middle stage
   - propagation delay
   - transition times

3) Output stage
   - Output characteristics
Figure 2.2.3: Bakhov's NAND gate macromodel

**INPUT STAGE:**

Nonlinear current sources, $J_A$ and $J_B$, and capacitances, $C_A$ and $C_B$, model the input characteristics of the device. The AND function is performed by taking the minimum of the input signals. This allows expansion of the macromodel into multiple inputs.

**MIDDLE STAGE:**

The voltage source $V_{\text{min}}$, resistance $R_1$, and macrocapacitance $W_1$ model the propagation delay of the gate. The macrocapacitance $W$ is defined as,

$$
C_w = \begin{cases} 
  f_1(V) & \text{for } \frac{dV}{dt} < 0 \\
  f_2(V) & \text{for } \frac{dV}{dt} > 0 
\end{cases}
$$

(2.2.1)

where: $V$ is the voltage across the macrocapacitance, a controlled voltage source $E(V)$. Assuming the delay in switching from logic 0 to logic 1 and logic 1 to logic 0 are equivalent, a macrocapacitance $W_1$ is used, which depends on the derivative of the voltage with respect to time.
The voltage source $E_1$, resistance $R_2$, and macrocapacitance $W_2$ model the transfer characteristic and the transition times of the gate. The macrocapacitance $W_2$ models the output signal edge rates when switching from logic 0 to logic 1 and from logic 1 to logic 0.

**Output Stage:**

The voltage source $E_2$, resistance $R_3$, capacitance $C_3$, and nonlinear current source $J_3$ model the output characteristics of the device. The voltage source $E_2$, which is a function of $W_2$, decouples the input from the output of the macromodel.

To increase the accuracy of the model, Bakhov suggests incorporating nonlinear voltage-controlled capacitances and nonlinear current sources at the input and the output of the model.

### 2.2.3 Summary

The macromodel examples are constructed based on three basic stages: an input stage, an internal stage, and an output stage. These three stages provide the operating characteristics of the device, namely:

- the input and output characteristics,
- the logic operation,
- the propagation delay, and
- the transition times of the device.

A comparison of the macromodel examples in relation to the four characteristics follows.
Nonlinear components provide an accurate model of the input characteristics of the device. The nonlinear current source in Glesner's model satisfactorily models the input characteristics. However, Bakhov's model, with a nonlinear current source and a shunt nonlinear capacitance, more accurately models the input characteristics.

The output characteristics of the models presented were modeled by simple, linear, lumped-element components. For improved accuracy, nonlinear components should be used to model the output characteristics. Bakhov suggests a series resistor with a shunt nonlinear current source and a shunt nonlinear capacitor. Glesner suggests a series nonlinear resistor with a shunt nonlinear current source and a shunt linear capacitor. Either output structure would provide reasonable accuracy. Although, a combination of both output structures, a series nonlinear resistor with a shunt nonlinear current source and a shunt nonlinear capacitor, would provide the best accuracy.

The logic operation of the device can be modeled by the voltage transfer characteristics in look-up table form or as a routine. In general, the voltage transfer characteristics are a function the output loading. Thus, the transfer characteristic provides only a first-order approximation to the logic operation under various output loads. Consequently, the voltage transfer characteristics accurately models the logic operation of the NAND gate.

A voltage source, resistor, and capacitor network model the transition times of the device. A routine can vary either the resistor or capacitor to simulate the different transition times which corresponds to the rise and fall times of the output signal.
Greenbaum does not model the transition times for the NAND gate.

A resistor, capacitor network or a delay routine can model the propagation delay of the device. Greenbaum uses a simple RC network to model the delay. Glesner's delay routine may provide more accuracy than the simple RC network.

With a slight modification of the input and output structures, Glesner's macromodel best represents the NAND gate. His techniques can be expanded to model other devices as well.

2.3 Definition of One-Port and Two-Port Macromodels

In developing macromodels of digital integrated circuits, the task is best accomplished by breaking down the macromodels into one-port and two-port models. The one-port models describe the input and output characteristics of the device. The two-port models describe the complete macromodel, including the input and output characteristics and the internal characteristics of the device.

2.3.1 One-Port Macromodels

The one-port macromodels describe the input and output characteristics of the device, which includes the input and output impedance and the current driving capabilities of the device. One-port macromodels are one terminal devices. Thus, the input or output characteristics are determined by looking into the device.

The input and output characteristics of the one-port device are a linear or nonlinear lumped-element model, consisting of resistors, capacitors, inductors, and voltage
or current sources. The voltage and current sources represent the current driving capabilities of the device. Some or all of the components can be nonlinear to accurately model the device for all voltage and frequency conditions. The nonlinear components can be represented by mathematical equations or look-up tables.

The component values of the lumped-element model are extracted from systematic DC and frequency-domain measurements of the device. DC I-V curves are used to extract the DC resistance of the device. In addition, voltage or current source values are determined from the DC measurements. Scattering parameters, a frequency-domain measurement, are used to extract the reactive components of the model.

A detailed discussion of one-port macromodels is presented in Chapter 3. Also, an example of one-port macromodels for a TTL NAND gate are presented.

2.3.2 Two-Port Macromodels

The two-port macromodel describes the complete device, which includes the input and output characteristics and the internal characteristics of the device. The two-port macromodel is a two terminal device. Thus, given a specific input, the output is known.

The two-port macromodel consists of an input stage, a delay stage, and an output stage. The input and output stage are determined from the one-port macromodels. The delay stage models the internal characteristics of the device, including the propagation delay and the logic operation. The delay stage is a linear lumped-element model, consisting of resistors, voltage-controlled sources, and a low-pass network.
The voltage-controlled source can be linear or nonlinear and can be represented by mathematical equations or look-up tables.

The component values of the lumped-element model are extracted from DC and transient measurements of the device. The voltage transfer characteristics are determined from a DC measurement of the device. The propagation delay is determined from a transient analysis or from a data book.

A detailed discussion of two-port macromodels is presented in Chapter 4. Also, an example of a two-port macromodel for a TTL NAND gate is presented.

2.4 Conclusion

This chapter has presented a review of macromodeling theory. The chapter was divided into two sections. First, a literature review was presented. The literature review discussed previous macromodeling work, several macromodel types, and three NAND gate macromodel examples. Second, an introduction to one-port and two-port macromodels was presented.

Previous macromodeling approaches included time-domain approaches, mathematical approaches, and lumped-element circuit behavioral approaches. The time-domain approach consisted of time-domain models based on a latent or a sensitivity approach to modeling a nonlinear device. The mathematical approach consisted of a system of differential and algebraic equations to model the device. The lumped-element behavioral modeling approach consisted of a simple lumped-element model with linear or nonlinear components. These approaches did not provide the computa-
tional speed increase and the accuracy needed for high-speed digital circuit simulation.

Three NAND gate macromodel examples were presented. The macromodels consisted of an input stage, an internal stage, and an output stage. The macromodels were lumped-element models which described the input and output characteristics, the logic operation, the propagation delay, and the transition times of the device.

An introduction to one-port and two-port macromodels was presented. The one-port macromodels described the input and output characteristics of the device. The two-port macromodels described the complete device, including the input and output characteristics and the internal characteristics of the device. The macromodels were constructed based on DC and scattering parameter measurements.
Chapter 3
Development of One-Port Macromodels

3.1 Introduction

In chapter 2, one-port and two-port macromodels were defined. This chapter presents a technique for developing the one-port macromodels. The input and output characteristics of TTL devices are discussed. As an example, the one-port macromodels of a FAST\(^1\) TTL NAND gate are developed. DC analysis and frequency-domain techniques for extracting the model components are presented. In addition, the calculation and optimization of the model components are presented.

The one-port macromodels describe the input and output impedance and the current driving capabilities of the device. The one-port macromodels are lumped-element models consisting of linear and nonlinear components. The components include resistors, inductors, capacitors, and current sources. The number and type of components used depends on the device being modeled.

The first step in developing a one-port macromodel is to understand the device being modeled. An assumed model is constructed based on the input and output structure of the device. Once the model is determined, the component values are calculated using DC and frequency-domain measurement techniques. DC measurement techniques are used to extract DC resistance and current source values of the model. Frequency-domain methods are used to extract reactive components of the model.

\(^{1}\)FAST is a registered trademark of Fairchild Semiconductor Corporation.
The model components may be nonlinear functions of voltage and frequency.

Two methods are presented for extracting model component values from measurements. First, a computer program provides a fast method for extracting the model component values. The equations describing the impedance and admittance of both the model and the actual device are solved for the component values as a function of frequency and voltage. Second, optimization provides an efficient method for extracting the model component values. Optimization is performed using a computer-aided design package which compares time or frequency-domain data of the model to those of the actual device. The model components are selected which provide the best match between the model data and the actual device data. These methods provide an estimate of the one-port macromodel's components.

### 3.2 Input and Output Characteristics of TTL Devices

The input and output characteristics describe the impedance and driving capabilities of the device. As an example of a one-port macromodel, consider a TTL device.
The assumed one-port macromodels for the device are shown in Figure 3.2.1. A series resistor, a series inductor, a shunt nonlinear resistor, and a shunt nonlinear capacitor model the input and output characteristics. A nonlinear current source is included with the output characteristics to model the driver characteristics of the device.

The series resistors, $R_{se}$ and $R_{so}$, model the lead resistances of the device package. In addition, the series inductors, $L_{si}$ and $L_{so}$, model the lead inductances of the device package. The series resistors and inductors are linear elements, independent of bias voltage. The shunt nonlinear capacitors, $C_i$ and $C_o$, model the input and output capacitances of the device. Likewise, the shunt nonlinear resistors, $R_i$ and $R_o$, model the input and output resistances of the device. The nonlinear resistors and the nonlinear capacitors are functions of DC bias voltage.

3.3 The FAST TTL NAND Gate Structure

Let us consider a specific example of a TTL digital device, the FAST TTL NAND gate, shown in Figure 3.3.1. The input structure consists of pn and Schottky diodes, current limiting resistors, and Schottky transistors. The output structure consists of the Schottky clamping diode, the "Miller Killer" circuitry, and the transistor totem-pole arrangement. The details of the input and output structures are presented as they relate to the nonlinear components of the one-port macromodel.

The nonlinear input resistance of the device is due to the input diodes and the current limiting resistor between the base and collector of $Q_1$. When the input voltages are low, gating diodes $D_1$ and $D_2$ are forward biased and the input resistance
Figure 3.3.1: FAST TTL NAND gate schematic [11]

is approximately equal to the 10 kΩ current limiting resistor at the base to collector of Q1. Otherwise, diodes D1 and D2 are reversed biased and the input resistance is large and is determined by diodes D1, D2, D3, and D4. At input voltages less than ground potential and above $V_{cc}$, clamping diodes D5 and D6 are forward biased and provide a low impedance path to ground. The clamping diodes serve to eliminate unwanted parasitics commonly found in bipolar integrated circuits and to provide high-speed dampening of reflections at the input [11]. The input resistance is bias voltage dependent. Therefore, the nonlinear input resistor of the model, $R_i$, models the change in the input current as a function of bias voltage.

The nonlinear input capacitance of the device is due to the junction capacitance
of diodes $D_1$, $D_2$, $D_3$, and $D_4$ and the base capacitance of transistors $Q_1$ and $Q_2$. Schottky diodes $D_3$ and $D_4$ remove the stored charge from the base of $Q_2$ on the negative transition of the input, thus speeding the positive transition of the output. Otherwise, the stored charge removal is limited to the base emitter resistor of $Q_2$ [11]. The input capacitance is bias voltage dependent. Therefore, the nonlinear input capacitor of the model, $C_i$, models the change in the input capacitance as a function of bias voltage.

The nonlinear output resistance of the device is due to the output resistance of the totem-pole arrangement of transistors $Q_3$ and $Q_6$ and the 45 $\Omega$ collector resistor of transistor $Q_6$. When the device is in the low state, transistor $Q_6$ is on and $Q_3$ is off, and current is sourced by the Darlington pair, $Q_5$ and $Q_6$. The output resistance is approximately $1/g_m$ of transistor $Q_6$, where $g_m$ is the transconductance of the transistor. When the device is in the high state, transistor $Q_2$ is on and $Q_6$ is off, and current is sunk to transistor $Q_3$. The output resistance is the output resistance of transistor $Q_3$, which is 50-100 k$\Omega$, in parallel with the load resistance. When the device is switching, both $Q_3$ and $Q_6$ are on, and the output resistance is approximately the 45 $\Omega$ collector resistor of transistor $Q_6$ in parallel with the load resistance. The output resistance is bias voltage dependent. Therefore, the nonlinear output resistor of the model, $R_o$, models the change in output current as a function of the state of the device.

The nonlinear output capacitance of the device is due to the totem-pole arrangement of transistors $Q_3$ and $Q_6$ and the “Miller Killer” circuitry. Transistor $Q_7$ and
diodes $D_9$, $D_{10}$, and $D_{11}$ comprise the "Miller Killer" circuitry. Since the output transistors $Q_3$ and $Q_8$ are required to conduct large currents, the transistors can not be fabricated with reduced geometry configuration. Consequently, transistor $Q_3$ has a large capacitance between the base and collector. Thus, the "Miller Killer" circuitry provides a low impedance current path to ground and removes excess charge from the base of $Q_3$ [11]. When the device is in the low state, the base-emitter capacitance of $Q_8$ comprises the output capacitance. When the device is in the high state, the collector-emitter and base-collector capacitance of transistor $Q_3$ comprise the output capacitance. Therefore, the nonlinear output capacitance of the model, $C_o$, models the change in output capacitance as a function of the state of the device.

3.4 Determination of the Input and Output Characteristics of the FAST TTL NAND Gate

Determination of the one-port macromodels of the FAST TTL device was a two-step process. First, the DC and scattering parameter measurements were taken with the device in a specified bias voltage range. The scattering parameters were de-embedded using a Through-Reflect-Line technique to remove the measurement errors [12]. Using microwave CAD software, the macromodel components were optimized such that the measured scattering parameters of the device fitted the scattering parameters of the one-port macromodel. The optimization provided an estimate of the one-port macromodel component values. Second, the model components were calculated at each bias voltage point from the scattering parameter measurements using a FORTRAN routine. Thus, the one-port macromodel components were obtained as a function of
bias voltage.

The input and output characteristics of the FAST TTL NAND gate were determined through systematic measurements of the input and output ports of the device. The nonlinear resistors of the macromodel (refer to Figure 3.2.1), $R_i$ and $R_o$, were determined from DC I-V curves of the device. The linear resistors, $R_{li}$ and $R_{lo}$, linear inductors, $L_i$ and $L_o$, and nonlinear capacitors, $C_i$ and $C_o$, were determined from scattering parameter measurements. The device was assumed to be unilateral, hence the input and output ports were independent of one another.

3.4.1 Determination of the Nonlinear Resistance of the Device Using I-V Measurements

The purpose of the I-V curve measurements was to extract the nonlinear input and output DC resistances of the device which correspond to the model resistors $R_i$ and $R_o$, respectively. The procedure was to apply a DC voltage to the input and the output of the device and to measure the corresponding current. Three measurements were taken: the input, the output in the low state, and the output in the high state. The measurements required a DC power supply, an ammeter, a voltmeter, and a test board containing the devices to be measured. To automate the measurements, a Hewlett-Packard programmable DC power supply was used. The measurement setup is shown in Figure 3.4.1.

For the input measurements, a range of DC voltages were applied to the input using the programmable power supply, and the corresponding current was read with an ammeter. The input voltage range was -1.0 to 6.0 volts. The measurements were
stored in a database for easy access. The data was plotted, and the resistance was estimated from the slope of the linear piecewise I-V curve. A plot of the input I-V curve is shown in Figure 3.4.2. The resistance was approximately 10 kΩ in the voltage range of -1.0 to 1.5 volts, approximately 1.5 kΩ in the threshold region of 1.5 to 1.8 volts, and approximately 100 kΩ in the voltage range of 1.8 to 6.0 volts. Therefore, an estimation of the nonlinear input resistance of the device was obtained as a function of DC bias voltage.

The output I-V measurements were taken for three cases: the device in the low state, the device in the high state, and the device switching. The procedure was similar to the input I-V measurements. One input of the device was designated a logic high, and the other input was either a logic low or logic high depending on the desired output state. For example, for the device in the low state, both inputs must
Input I-V Curve of TTL NAND Gate

Figure 3.4.2: Plot of input I-V curve of 74F00 TTL NAND gate device
be high, and for the device in the high state, one input was low and one high. In addition, for the case in which the device was switching, the input voltage was set in the threshold region.

The output I-V measurements were taken by applying the DC voltage directly to the output and measuring the corresponding current. Again, the data was plotted, and the resistance was estimated from the slope of the linear piecewise I-V curve. A plot of the output low I-V curve and the output high I-V curve are shown in Figures 3.4.3 and Figure 3.4.4, respectively. For the output in the low state, the resistance was large in the range of -1.0 to 2.0 volts, approximately 15 $\Omega$ in the voltage range of 2.0 to 3.5 volts, and approximately 50 $\Omega$ in the voltage range of 3.5 to 6.0 volts. For the output in the high state, the resistance was approximately 50 $\Omega$ in the voltage range of -1.0 to 3.5 volts and approximately 100 k$\Omega$ in the voltage range of 3.5 to 6.0 volts. Therefore, an estimation of the nonlinear output resistance was obtained as a function of the state of the device.

3.4.2 Determination of the Lead Resistance, Lead Inductance, and the Nonlinear Capacitance of the Device

The input and output lead resistance, lead inductance, and nonlinear capacitance of the device were estimated from scattering parameter measurements. From the scattering parameters, the impedance of the device was calculated, and thereby the lead resistance, lead inductance, and capacitance as a function of bias voltage was determined from equations which represent a physical model of the device. Furthermore, optimization was performed on the measured scattering parameters of the device and
Figure 3.4.3: Plot of output I-V curve of 74F00 TTL NAND gate with the device in the low state
Figure 3.4.4: Plot of output I-V curve of 74F00 TTL NAND gate with the device in the high state.
the scattering parameters of the model using TOUCHSTONE, a microwave design CAD tool [13].

3.4.3 Scattering Parameter and Transmission Line Background

Scattering parameters are a linear relationship between the incident and reflected traveling waves of a network. Scattering parameters are useful at microwave frequencies in which traditional network measurements involving short and open circuits can not be utilized. The problems with traditional network measurements at microwave frequencies are threefold [14]:

- equipment is not readily available to measure total voltages and total currents for multi-port networks,

- short and open circuits are difficult to achieve, and

- measurement instabilities exist associated with short and open circuits.

Consequently, the solution is to use traveling waves rather than total voltages and total currents at microwave frequencies. Figure 3.4.5 shows the voltage traveling waves for a general two-port network. The voltage source $V_s$, source impedance $Z_s$, and load impedance $Z_l$ is connected to the two-port network via a transmission line of characteristic impedance $Z_c$. The scattering parameters are related to the voltage traveling waves by [15],

$$V_1^- = S_{11}V_1^+ + S_{12}V_2^+$$ (3.4.1)
\[ V_2^- = S_{21}V_1^+ + S_{22}V_2^+ \quad (3.4.2) \]

If port two is terminated in a matched load, such that \( Z_c = Z_L \), then \( V_2^+ \) is zero (no reflection) and (3.4.1) reduces to

\[ S_{11} = \frac{V_1^-}{V_1^+} \quad (3.4.3) \]

and (3.4.2) reduces to

\[ S_{21} = \frac{V_2^-}{V_1^+} \quad (3.4.4) \]

Similarly, if port one is terminated in a matched load, then \( V_1^+ \) is zero and (3.4.2) reduces to

\[ S_{22} = \frac{V_2^-}{V_2^+} \quad (3.4.5) \]

and (3.4.1) reduces to

\[ S_{12} = \frac{V_1^-}{V_2^+} \quad (3.4.6) \]

Therefore, \( S_{11} \) and \( S_{22} \) are equivalent to the reflection coefficients at ports one and two, respectively, and \( S_{21} \) and \( S_{12} \) are equivalent to the forward and reverse voltage gain, respectively.
From transmission line theory, the input impedance of a transmission line is a function of the characteristic impedance of the line and the reflection coefficient [16]. In general, this applies to any passive one-port device as well. Since the reflection coefficient has already been defined in terms of \( S_{11} \) and \( S_{22} \), the input and output impedances of the device can be determined from scattering parameter measurements. Thus, the measured input and output impedances are given by (3.4.7) and (3.4.8), respectively.

\[
Z_{in} = Z_c \left( \frac{1 + S_{11}}{1 - S_{11}} \right) = R_{in} + jX_{in} \tag{3.4.7}
\]

\[
Z_{out} = Z_c \left( \frac{1 + S_{22}}{1 - S_{22}} \right) = R_{out} + jX_{out} \tag{3.4.8}
\]

Once the input and output impedance of the device is known, the equivalent lumped-element one-port macromodels can be constructed.

### 3.4.4 Calculation of Model Components From Scattering Parameter Measurements

At this point, the nonlinear resistors of the model in Figure 3.2.1, \( R_i \) and \( R_o \), have been determined. The remaining model components, the series resistors, series inductors, and nonlinear capacitors, were determined from scattering parameter measurements. The procedure was as follows:

- calculate the nonlinear capacitors from the measured input and output susceptance of the device calculated from \( S_{11} \) and \( S_{22} \),

- calculate the series inductors from the measured input and output reactance of the device calculated from \( S_{11} \) and \( S_{22} \), and
• calculate the series resistors from the measured input and output resistance of
  the device calculated from $S_{11}$ and $S_{22}$.

All of the model components were assumed to be independent of frequency. In ad-
dition, the series resistors and series inductors of the model were independent of
bias voltage, and the nonlinear resistors and nonlinear capacitors of the model were
functions of bias voltage.

The nonlinear capacitors of the model, $C_i$ and $C_o$, were calculated from the mea-
sured input and output admittance of the device, respectively. At low frequencies, the
impedance due to the series inductors was assumed negligible, thus the capacitance
was calculated directly from the measured admittance of the device. From (3.4.9) and
(3.4.11), the input and output admittances were determined from measured values
of $S_{11}$ and $S_{22}$, respectively. Furthermore, from (3.4.10) and (3.4.12), the input and
output capacitances were calculated from the input and output susceptances.

\[
Y_{\text{in}} = \frac{1}{Z_{\text{in}}} = Y_e \left( \frac{1 - S_{11}}{1 + S_{11}} \right) = G_{\text{in}} + jB_{\text{in}} \quad (3.4.9)
\]

\[
C_i (V) = \frac{B_{\text{in}}}{\omega} \quad (3.4.10)
\]

\[
Y_{\text{out}} = \frac{1}{Z_{\text{out}}} = Y_e \left( \frac{1 - S_{22}}{1 + S_{22}} \right) = G_{\text{out}} + jB_{\text{out}} \quad (3.4.11)
\]

\[
C_o (V) = \frac{B_{\text{out}}}{\omega} \quad (3.4.12)
\]

where: $Y_{\text{in}} \equiv$ input admittance

$Y_{\text{out}} \equiv$ output admittance

$Y_e \equiv$ characteristic admittance

$G_{\text{in}} \equiv$ input conductance

$B_{\text{in}} \equiv$ input susceptance
\[ G_{\text{out}} = \text{output conductance} \]
\[ B_{\text{out}} = \text{output susceptance} \]
\[ \omega = \text{angular frequency (}2\pi f\text{)} \]

The input and output capacitors were calculated over a range of bias voltages from 0.0 to 5.0 volts at a frequency of 10 MHz.

The series inductors of the model, \( L_i \) and \( L_o \), were calculated from the measured input and output impedances of the device, respectively. The input and output impedances were determined from \( S_{11} \) and \( S_{22} \) at a frequency of 1 GHz, in which the impedance due to the inductance dominates the impedance due to the capacitance. Equation (3.4.7) of section 3.4.3 provided the measured input impedance of the device as a function of the measured values of \( S_{11} \). Equation (3.4.13) provided the analytical input impedance of the model determined from Figure 3.2.1.

\[
Z_{\text{in}} = R_i + \frac{R_i}{1 + (\omega R_i C_i)^2} + j\omega \left( L_i - \frac{R_i^2 C_i}{1 + (\omega R_i C_i)^2} \right) \quad (3.4.13)
\]

Provided the calculations of the resistance and capacitance were correct, equating the imaginary parts of (3.4.7) and (3.4.13) and solving for the input inductance of the model \( L_i \) gives,

\[
L_i = \frac{X_{\text{in}}}{\omega} + \frac{R_i^2 C_i}{1 + (\omega R_i C_i)^2} \quad (\omega \neq 0) \quad (3.4.14)
\]

where:
- \( X_{\text{in}} \equiv \text{measured input reactance of device} \)
- \( R_i \equiv \text{nonlinear input resistance of model} \)
- \( C_i \equiv \text{nonlinear input capacitance of model} \)
- \( L_i \equiv \text{series input inductance of model} \)

Analogous to the input inductance, the output inductance, \( L_o \), was determined by equating the measured output reactance of the device with the output reactance
of the model, shown in (3.4.15).

\[ L_o = \frac{X_{out}}{\omega} + \frac{R_o^2 C_o}{1 + (\omega R_o C_o)^2} \quad (\omega \neq 0) \]  

(3.4.15)

where:  
\( X_{out} \equiv \) measured output reactance of device  
\( R_o \equiv \) nonlinear output resistance of model  
\( C_o \equiv \) nonlinear output capacitance of model  
\( L_o \equiv \) series output inductance of model

The input and output series inductors were calculated over a range of bias voltages from 0.0 to 5.0 volts at a frequency of 1 GHz. The series inductors were linear, independent of bias voltage.

The input and output series resistors of the model, \( R_{ni} \) and \( R_{no} \), were calculated from the measured input and output impedances of the device, respectively. The measured input impedance of the device and the analytical input impedance of the model were given by (3.4.7) and (3.4.13), respectively. Provided the nonlinear resistance and nonlinear capacitance calculations are correct, equating the real parts of (3.4.7) and (3.4.13) and solving for the series resistance of the model \( R_{ni} \) gives,

\[ R_{ni} = R_{in} - \frac{R_i}{1 + (\omega R_i C_i)^2} \]  

(3.4.16)

where:  
\( R_{in} \equiv \) measured input resistance of device  
\( R_i \equiv \) nonlinear input resistance of model  
\( C_i \equiv \) nonlinear input capacitance of model

Analogous to the input series resistance, the output series resistance, \( R_{no} \), was determined by equating the measured output resistance of the device with the output
resistance of the model, shown in (3.4.17).

\[ R_{so} = R_{out} - \frac{R_o}{1 + (\omega R_o C_o)^2} \]  \hspace{1cm} (3.4.17)

where:
- \( R_{out} \equiv \) measured output resistance of device
- \( R_o \equiv \) nonlinear output resistance of model
- \( C_o \equiv \) nonlinear output capacitance of model

The input and output series resistors were calculated over a range of bias voltages from 0.0 to 5.0 volts at frequencies of 10 MHz and 1 GHz. The series resistors were linear, independent of bias voltage.

3.4.5 Optimization of Model Components

In the previous section, the model components for a FAST TTL device were calculated from measured scattering parameters using a FORTRAN program. The calculations provided an estimation of the model components from measured scattering parameters of an actual device. To ensure the correctness of the model component values, optimization was performed on the measured scattering parameters of the device and the scattering parameters of the assumed one-port macromodels for the FAST TTL device.

TOUCHSTONE, a CAD software package which performs linear analysis, interactive tuning, and optimization of RF and microwave circuits, was used to perform the optimization [13]. TOUCHSTONE optimized the macromodel components such that the measured scattering parameters of the device fitted the scattering parameters of the one-port macromodel. The optimization consisted of minimizing an error
function, defined in terms of the measured scattering parameters of the device and the scattering parameters of the model, by adjusting the macromodel components.

Optimization was performed on the input and output one-port macromodels for the scattering parameter files corresponding to several applied bias voltages. The bias voltage range was 0 to 5 volts, and the scattering parameters were optimized over a frequency range of 45 MHz to 1 GHz. The optimized model components agreed well with the calculated model components using the FORTRAN program.

3.5 Conclusion

This chapter presented techniques for developing one-port macromodels. The one-port macromodels modeled the input and output characteristics and the current driving capabilities of the device. A series resistor, a series inductor, a shunt nonlinear resistor, and a shunt nonlinear capacitor modeled the input and output characteristics of a FAST TTL device.

The macromodel components were calculated from DC I-V curve measurements and scattering parameter measurements. The shunt nonlinear resistors were calculated from the slope of the I-V curves. The series resistors, series inductors, and nonlinear capacitors were calculated from scattering parameter measurements. The measured impedance and admittance were calculated from scattering parameter measurements, and the macromodel components were calculated by equating the measured impedance and admittance of the device to the impedance and admittance of the macromodel.
Two methods were used to calculate the macromodel components. First, a FORTRAN computer program was used to calculate the macromodel components by comparing the measured impedance of the device to the analytical impedance of the macromodel. Second, optimization was used to calculate the one-port macromodel components. Using a CAD software program, the macromodel components were optimized such that the measured scattering parameters of the device fitted the scattering parameters of the assumed one-port macromodel.
Chapter 4

Development of Two-Port Macromodels

4.1 Introduction

In Chapter 3, a technique for developing one-port macromodels was presented. The one-port macromodels described the input and output characteristics of the device. The input and output characteristics are an essential part of the macromodel, however, a digital device is a two-port device. Two-port functionality includes the internal characteristics of the device, such as logic operation, propagation delay, noise immunity, temperature effects, and input coupling. In order to model these additional effects, and thus provide a working macromodel of the digital device, the one-port macromodel must be expanded into a two-port macromodel.

The purpose of the two-port macromodel is to provide a functional time-domain model of a digital device with a factor of five to ten computational speed increase over a transistor-level model of the device. The two-port macromodel closely models the actual device including nonlinear input and output impedance, current drive capabilities, logic operation, propagation delay, and ground noise. The two-port macromodel is SPICE compatible and can be implemented in a transmission line simulator for studying high-speed propagation of digital signals.
4.2 Defining the Internal Characteristics of the Device

As stated earlier, the purpose of the two-port macromodel is to provide a complete model of a digital integrated circuit. The digital integrated circuit is a complex device. It is nearly impossible for the macromodel to completely model the device in every aspect. Rather, the macromodel provides a time-domain approximation of the digital device which is within 10 to 20 percent of the actual device.

The internal characteristics of the two-port macromodel include current drive capability, logic operation, propagation delay, and ground noise. These internal characteristics are necessary for a functional time-domain macromodel. All other second-order effects, such as temperature dependence, input coupling, etc. will be assumed negligible.

4.2.1 Current Drive Capability

The current drive capability of a digital integrated circuit is a function of the output characteristics of the device and the output loading conditions. The output characteristics of the device consist of a Thevenin equivalent circuit, comprised of a nonlinear voltage-controlled voltage source in series with a linear resistor. This configuration provides the output current drive of the device. Either a Thevenin or a Norton equivalent circuit can be used for the output characteristics, since the nonlinear Thevenin equivalent circuit behaves identically to a nonlinear Norton equivalent circuit. However, a Thevenin equivalent circuit provides better SPICE convergence.
4.2.2 Logic Operation

The logic operation of a digital integrated circuit describes the output voltage as a function of the input voltages. As an example, consider a common IC, the NAND gate. From digital logic design, the NAND gate is comprised of an inverter and an AND gate. The Boolean algebra expression and the truth table for the NAND gate are shown in Figure 4.2.1. Boolean algebra is a special branch of algebra applicable to the binary system which is useful for the logic and circuit designer in designing and using digital integrated circuits. The truth table is a listing of the values for the dependent variable versus all of the corresponding values of the independent variables [17]. Therefore, for the NAND gate, the output is high for all combinations of the input voltages except when both inputs are high, in which the output is low.

The logic operation of the NAND gate macromodel is modeled by voltage-controlled voltage sources. The output stage consists of two nonlinear voltage-controlled voltage sources which are functions of the input voltages. In addition, the output stage
consists of two switches which are functions of the input voltages. The switches ensure the correct output impedance and current drive as a function of the state of the device. The input stage consists of an impedance network, which models the input impedance of the device. Although the 74F00 NAND gate is a dual input device, the NAND gate macromodel is a single input device with one input tied high. This provides a simpler input stage and ensures that all logic output states are achieved for all possible inputs.

4.2.3 Propagation Delay

The propagation delay of a digital IC is defined as the delay between a signal applied to the input of the device and the corresponding signal at the output of the device. The propagation delay exists due to the RC time constants in the circuit. These RC time constants consist of the equivalent resistance seen by the circuit and the finite charging and discharging times of the capacitors in the circuit. The total propagation delay is the average of the low-to-high transition time, \( t_{pLH} \), when the output is changing from LOW to HIGH, and the high-to-low transition time, \( t_{pHL} \), when the output is changing from HIGH to LOW [17]. The two propagation delays are shown in Figure 4.2.2.

The propagation delay can be modeled in one of two ways: as an equivalent resistor-capacitor network, or as a transmission line. The resistor-capacitor (RC) network consists of a resistor in parallel with a capacitor. The transmission line consists of a distributed low-pass network with a characteristic impedance and a
finite delay time.

The resistor-capacitor network provides a low-pass network with a delay time equivalent to the RC time constant. The RC delay network is shown in Figure 4.2.3. For example, a 100 Ω resistor in parallel with a 20 pF capacitor has an equivalent RC time constant of 100 Ω × 20 pF = 2 ns. Hence, the time constant serves to delay the output signal by 2 ns. The advantages of the RC network are that it is simple to implement, and it has fast convergence. The disadvantage of the RC network is that large RC time constants distort the time-domain output pulse and reduce accuracy. Thus, only small delays are possible without noticeable distortion and degradation of the output pulse.

A matched transmission line can also model the propagation delay of the device.
The transmission line delay network is shown in Figure 4.2.4. The transmission line is considered matched when the characteristic impedance $Z_e$ is equal to the load impedance $R_d$ of the line. The characteristic impedance of the transmission line is a ratio of the voltage to the current at any point on the line. The time delay of the transmission line is a function of the line length and the propagation velocity of the signal. The advantage of a transmission line delay network is that it is accurate and does not distort the output pulse. The disadvantage of a transmission line delay network is that it has slow convergence, especially for short lines. A small delay requires a short transmission line which requires small time steps and results in long run times. SPICE provides a lossless transmission line model which requires the characteristic impedance of the line, $Z_e$, and the time delay of the line, $t_d$. 
4.2.4 Ground Noise

Ground noise results from both power supply current transients and signal return current transients. Transient currents on the ground return path are largely due to transistors switching states. The transient currents cause significant voltage drops in the ground return path due to the ground inductance. The ground inductance consists of the ground plane-to-device interconnection on a printed circuit board and the lead inductance of the device package. As clock speeds and rise times increase, ground noise becomes a necessary consideration in digital circuit design. For more information on ground noise, refer to Appendix A.

The NAND gate macromodel models the ground noise of the device. All model components are referenced to a ground inductor. The ground inductor models the lead inductance of the device package and provides a good estimation of the ground noise in the device. In addition, series inductors are placed at the input and output stages of the model to model the lead inductance of the input and output bond wires.
4.3 Conclusion

This chapter presented techniques for developing two-port macromodels. The two-port macromodel provided a functional time-domain model of a digital integrated circuit with a factor of five to ten speed increase over the transistor-level model of the device. The two-port macromodel modeled both the external characteristics and the internal characteristics of the device. The internal characteristics included the current drive capabilities, the logic operation, the propagation delay, and the ground noise.

The current drive capabilities were modeled by a nonlinear Thevenin equivalent circuit consisting of a nonlinear voltage-controlled voltage source in series with a linear resistor. The logic operation was modeled by voltage-controlled voltage sources at the delay stage and the output stage. The propagation delay was modeled by a low-pass network consisting of either a RC network or a lossless transmission line. The ground noise is modeled by inductors. All model components are referenced to a ground inductor, and series inductors are placed at the input and output stages to model the lead inductance of the device package.
Chapter 5

Development of 74F00 NAND Gate Macromodel

5.1 Introduction

Chapters 3 and 4 presented techniques for developing one-port and two-port models of digital integrated circuits. In this chapter, a 74F00 NAND gate macromodel is constructed based on the techniques presented in Chapters 3 and 4. The 74F00 is a dual-input, positive logic, FAST TTL NAND gate device. Scattering parameter results are presented for the one-port macromodels. In addition, problems and limitations of the macromodel are discussed.

The results consist of a comparison of the measured scattering parameters of the device to the simulated scattering parameters of the one-port macromodel. Tables of the linear and nonlinear model components corresponding to the simulated scattering parameters are presented. Results are presented for several applied bias voltages for both the input and output one-port macromodels.

The objective of the 74F00 macromodel is to provide a functional time-domain model of the 74F00 device with a factor of 5 to 10 computational speed increase over the corresponding transistor-level model. The macromodel is implemented in PSpice\(^1\), a commercial analog circuit simulator, for performing high-speed digital circuit simulations. A PSpice circuit file listing is included.

\(^1\)PSpice is a registered trademark of MicroSim Corporation
5.2 Implementation of the Two-Port NAND Macromodel

The complete two-port macromodel of a 74F00 NAND gate is implemented in PSpice, an analog circuit simulator [18]. PSpice provides more features than the Berkeley version of SPICE, including table look-up of controlled sources, dependent sources described by equations, nonlinear voltage and current controlled switches, and analog behavioral modeling. Although the macromodel is implemented in PSpice, it can be modified to work in a standard Berkeley SPICE version as well.

The macromodel consists of three stages: the input stage, the delay stage, and the output stage. The input stage models the input characteristics of the device. The delay stage models the propagation delay of the device. The output stage models the output characteristics and the logic operation of the device. The complete 74F00 macromodel is shown in Figure 5.2.1. The SPICE circuit file and user's guide for the macromodel are presented in Appendix C.

5.2.1 Input Stage

The input stage consists of a series resistor, a series inductor, a shunt nonlinear resistor, and a shunt capacitor. In general, the 74F00 is a dual-input device, however, for simplicity, the macromodel is designed as a single-input device with the second input tied to a high level ($V_{cc}$). This ensures all possible output states for a low-to-high input transition. The macromodel can be modified to include dual-inputs if desired.

As discussed in Chapter 3, the linear series resistor, $R_{si}$, and the linear series
inductor, $L_i$, model the lead resistance and the lead inductance of the device package, respectively. An average value of 15 $\Omega$ is used for $R_{si}$, and an average value of 2 nH is used for $L_i$. The model component values are calculated from scattering parameter measurements, using the techniques described in Chapter 3.

The shunt capacitor, $C_i$, models the input capacitance of the device. The capacitor is linear and an average value of 5 pF is used for the model. A nonlinear capacitor provides better accuracy for the input characteristics, but PSpice does not provide a nonlinear capacitor model. The linear capacitor provides a good approximation since the input capacitance does not deviate much over the voltage range of 0.0 to 5.0 volts. For more information on nonlinear capacitors, refer to Appendix B.

The shunt nonlinear resistor, $R_i$, models the input resistance of the device. The nonlinear resistor is implemented in the form of a look-up table in PSpice. The
table corresponds to the DC I-V curves taken from the actual device. Thus, the nonlinear resistor ensures the correct input resistance over the input voltage range. The input I-V curve for the device is shown in Chapter 3. Although SPICE does not provide a nonlinear resistor explicitly, the nonlinear resistor can be implemented using a nonlinear voltage-controlled current source. For more information on nonlinear resistors, refer to Appendix B.

The macromodel elements are estimated by fitting the measured scattering parameters of the device with the scattering parameters of the macromodel. The measured scattering parameter results for the input of the device as a function of applied input bias are shown in Figure 5.2.2. The plots include the magnitude and phase of $S_{11}$. Six cases are presented corresponding to bias voltages of 0, 1, 2, 3, 4, and 5 volts. The magnitude of $S_{11}$ is fairly smooth except for the 0 bias voltage case. $S_{11}$ for the 0 volt case oscillates over the entire frequency range of 45 MHz to 1 GHz. This is probably due to measurement errors and noise. The phase of $S_{11}$ is smooth for all the bias voltage cases over the entire frequency range.

In addition, the optimized $S_{11}$ values of the macromodel and the measured $S_{11}$ values of the device are presented for each bias voltage case. Figures 5.2.3, 5.2.4, 5.2.5, 5.2.6, 5.2.7, and 5.2.8 present the $S_{11}$ magnitude and phase results for applied input bias voltages of 0, 1, 2, 3, 4, and 5, respectively. Table 5.2.1 presents the optimized model component values for each bias voltage case. Good agreement is obtained.
Figure 5.2.2: Magnitude and phase of measured $S_{11}$ for the 74F00 device versus applied input bias voltage. Symbols corresponding to bias voltages are: 0 V — $\diamond$, 1 V — $\ast$, 2 V — $\Delta$, 3 V — $+$, 4 V — $o$, and 5 V — $\times$. 
Figure 5.2.3: Magnitude and phase of measured $S_{11}$ (——) for the 74F00 device and optimized $S_{11}$ (----) for the macromodel at an applied input bias voltage of 0 volts.
Figure 5.2.4: Magnitude and phase of measured $S_{11}$ (——) for the 74F00 device and optimized $S_{11}$ (---) for the macromodel at an applied input bias voltage of 1 volts.
Figure 5.2.5: Magnitude and phase of measured $S_{11}$ (solid) for the 74F00 device and optimized $S_{11}$ (dashed) for the macromodel at an applied input bias voltage of 2 volts.
Figure 5.2.6: Magnitude and phase of measured $S_{11}$ (——) for the 74F00 device and optimized $S_{11}$ (---) for the macromodel at an applied input bias voltage of 3 volts.
Figure 5.2.7: Magnitude and phase of measured $S_{11}$ (——) for the 74F00 device and optimized $S_{11}$ (-----) for the macromodel at an applied input bias voltage of 4 volts.
Figure 5.2.8: Magnitude and phase of measured $S_{11}$ (-----) for the 74F00 device and optimized $S_{11}$ (-----) for the macromodel at an applied input bias voltage of 5 volts.
Table 5.2.1: Macromodel component values for input stage as a function of applied bias voltage

<table>
<thead>
<tr>
<th>Bias Voltage (V)</th>
<th>R_m (Ω)</th>
<th>L_i (nH)</th>
<th>R_i (Ω)</th>
<th>C_i (pF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>15</td>
<td>2.8</td>
<td>280</td>
<td>5.5</td>
</tr>
<tr>
<td>1</td>
<td>15</td>
<td>2.8</td>
<td>10k</td>
<td>4.6</td>
</tr>
<tr>
<td>2</td>
<td>15</td>
<td>2.8</td>
<td>1.5k</td>
<td>4.4</td>
</tr>
<tr>
<td>3</td>
<td>15</td>
<td>2.8</td>
<td>225k</td>
<td>4.0</td>
</tr>
<tr>
<td>4</td>
<td>15</td>
<td>2.8</td>
<td>150k</td>
<td>3.8</td>
</tr>
<tr>
<td>5</td>
<td>15</td>
<td>2.8</td>
<td>150k</td>
<td>3.8</td>
</tr>
</tbody>
</table>

5.2.2 Delay Stage

The delay stage consists of a voltage-controlled voltage source, \( E_d \), a lossless transmission line, \( T_d \), and a shunt resistor, \( R_d \). The voltage-controlled voltage source transfers the output voltage of the input stage to the delay stage. The lossless transmission line models the delay of the input voltage. The shunt resistor provides proper termination of the transmission line to ensure signal integrity.

The voltage-controlled voltage source, \( E_d \), is a linear dependent voltage source. Its purpose is to transfer the output voltage of the input stage to the delay stage. The SPICE command consists of the source nodes, the controlling nodes and a gain factor. The gain factor is the voltage gain between the source voltage and the controlling voltage. For example, if the gain factor is 10, then the source voltage is ten times larger than the controlling voltage. Since the voltage-controlled voltage source \( E_d \) merely transfers the voltage between the input and delay stages, the gain factor is one.

The transmission line, \( T_d \), is a lossless delay line. Terminated correctly with source
and load resistors, the transmission line models an ideal delay line. SPICE provides a lossless transmission line model. The parameters required are the characteristic impedance of the line and the time delay. Hence, if a 2 ns delay time is desired, then the time delay parameter is set to 2 ns. The characteristic impedance enables impedance matching between the transmission line, the source, and the load. Both the characteristic impedance and the terminating resistor are chosen to be 50 Ω. The 50 Ω value is arbitrary and any value could be used, as long as the characteristic impedance and the terminating resistor values are the same. In addition, the source resistance is zero (a short), sourcing the input voltage to the line.

The terminating resistor, \( R_d \), is a linear resistor which provides a matching load for the transmission line and transfers the output voltage of the delay network to the output stage. \( R_d \) is chosen to be 50 Ω, equal to the characteristic impedance of the transmission line, \( T_d \). A time delay exists between the voltage-controlled voltage source, \( E_d \), and the voltage across \( R_d \), which is transferred to the output stage.

### 5.2.3 Output Stage

The output stage consists of nonlinear voltage-controlled voltage sources, \( E_{ol} \) and \( E_{oh} \), linear resistors, \( R_{ol} \) and \( R_{oh} \), linear capacitors, \( C_{ol} \) and \( C_{oh} \), nonlinear voltage-controlled switches, \( S_{ol} \) and \( S_{oh} \), a linear series resistor, \( R_o \), and a linear series inductor, \( L_o \). The output stage consists of two sections: an output low and an output high. The output low section and the output high section model the current driving capabilities and output impedance under the output low state and the output high
state, respectively.

The voltage-controlled voltage sources are nonlinear dependent voltage sources, which model the current drive capability of the device as a function of the output state. $E_{cl}$ and $E_{ch}$ model the voltage transfer characteristics for the output low state and output high state, respectively. $E_{cl}$ and $E_{ch}$ are determined by taking the Thevenin equivalent voltage transfer characteristics from measurements or a simulation. The output voltage is measured under open circuit conditions (unloaded) at the output of the device, while the input is swept in a voltage range of -1.0 to 6.0 volts. A look-up table is created for each voltage-controlled source, $E_{cl}$ and $E_{ch}$, consisting of the output voltage as a function of the input voltage of the device. Both voltage-controlled voltage sources are a function of the output voltage at the delay stage.

The linear resistors model the output resistance as a function of the output state of the device. The resistor values are determined from the output I-V curves of the device. Since the resistors are linear, an average value of resistance is used for each resistor, which is verified by a transistor-level model simulation. $R_{cl}$ and $R_{ch}$ model the output resistance for the output low state and the output high state, respectively. The resistor values used for $R_{cl}$ and $R_{ch}$ are 50 $\Omega$ and 10 k$\Omega$, respectively. The choice of resistor values provide good agreement between the output characteristics of the macromodel and the actual device. The output characteristics of the macromodel can be improved by using nonlinear resistors substituted for the linear resistors. The nonlinear resistors consist of the output I-V curves for the device. Due to convergence problems, linear resistors are used for the macromodel's output stage.
The linear capacitors model the output reactance as a function of the output state of the device. The capacitor values are determined from an average value of capacitance calculated from scattering parameter measurements over a specified voltage range. $C_{ol}$ and $C_{oh}$ model the output capacitance for the output low state and the output high state, respectively. A value of 5 pF is used for $C_{ol}$ and 10 pF is used for $C_{oh}$. The linear capacitors are a good approximation to the nonlinear capacitance of the actual device.

The nonlinear voltage-controlled switches model the logic operation and output characteristics as a function of the output state of the device. The switches are nonlinear resistors controlled by the input voltage of the device. The switches provide the logic operation and the correct output impedance by opening or shorting the appropriate output circuitry. $S_{ol}$ functions as a short circuit when the output is in the low state and functions as an open circuit when the output is in the high state. Similarly, $S_{oh}$ functions as a short circuit when the output is in the high state and functions as an open circuit when the output is in the low state. The resistance values of the switch range from 1 Ω, approximating a short circuit, to 100 kΩ, approximating an open circuit. In addition, turn on and turn off voltages are specified for the switches. The controlling voltage is the output voltage of the delay stage.

The linear output series resistor, $R_{oe}$, and linear output series inductor, $L_o$, model the lead resistance and lead inductance of the device package, respectively. The components' values are calculated from scattering parameter measurements, using
Table 5.2.2: Macromodel component values for output stage as a function of the state of the device

<table>
<thead>
<tr>
<th>Output State</th>
<th>$R_m$ ($\Omega$)</th>
<th>$L_1$ (nH)</th>
<th>$R_i$ ($\Omega$)</th>
<th>$C_i$ (pF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>low</td>
<td>20</td>
<td>2.6</td>
<td>62</td>
<td>12</td>
</tr>
<tr>
<td>high</td>
<td>20</td>
<td>2.6</td>
<td>10k</td>
<td>5</td>
</tr>
</tbody>
</table>

The techniques described in Chapter 3. An average value of 15 $\Omega$ is used for $R_m$, and an average value of 3 nH is used for $L_1$.

The macromodel elements are estimated by fitting the measured scattering parameters of the device with the simulated scattering parameters of the macromodel. Scattering parameter results are presented for the output low and output high state of the device in Figures 5.2.9 and 5.2.10, respectively. The results include the magnitude and phase of the measured $S_{22}$ values of the device and the simulated $S_{22}$ values of the macromodel as a function of frequency. For the output high state, the measured magnitude of $S_{22}$ deviates as much as 2 dB over the frequency range of 45 MHz to 1 GHz. The optimized magnitude of $S_{22}$ approximates the measured magnitude of $S_{22}$ over the frequency range. The phase agreement is good except for a slight phase shift. For the output low state, the measured value of $S_{22}$ agrees well with the optimized value of $S_{22}$. Table 5.2.2 presents the optimized model component values for the output low and output high state of the device.
Figure 5.2.9: Magnitude and phase of measured $S_{22}$ (——) for the 74F00 device and optimized $S_{22}$ (---) for the macromodel with the output in the low state. Bias voltage of 4 volts applied to the input of the device.
Figure 5.2.10: Magnitude and phase of measured \( S_{22} \) (-----) for the 74F00 device and optimized \( S_{22} \) (-----) for the macromodel with the output in the high state. Bias voltage of 0 volts applied to the input of the device.
5.2.4 Ground Noise Modeling

The ground noise is modeled by a linear inductor, $L_g$. All model components are referenced to the ground inductor. An accurate value for the ground noise inductance is difficult to obtain in practice. The amount of inductance depends on the mounting environment, such as a breadboard or a printed circuit board, the size of the device package, and the configuration of the pins. The larger the package, the longer the bond wires, thus, the greater the inductance. Signetics has done some work on estimating the bond wire inductance [19]. For a 16-pin package, the ground inductance is estimated to be approximately 10 nH. Therefore, an approximate value of 10 nH is used for $L_g$. For more information on ground noise, refer to Appendix A.

5.3 Problems and Limitations of Model

The macromodel provides a good model of a 74F00 NAND gate device. However, there are problems with the model due to approximations and analog circuit simulator limitations. The problems and limitations include: the single-input stage, the linear output resistors, the linear input and output capacitors, and convergence problems.

5.3.1 Single-Input Stage

The 74F00 NAND gate is a dual-input device. For simplicity, the macromodel is constructed as a single-input device, with the second input assumed to be tied to a high voltage level. However, the macromodel's input stage can be modified to include dual-inputs. There are two ways in which the input stage can be modified. First,
Figure 5.3.1: Dual-input stage with a voltage-controlled voltage source

A second input is created with the same form as the first input, and both inputs are connected via a voltage-controlled voltage source. The voltage-controlled voltage source monitors the difference in voltage of the two inputs and sends the result to the delay stage. The dual-input structure is shown in Figure 5.3.1.

Second, a dual-input diode model can be used, shown in Figure 5.3.2. The dual-input diode model resembles the input stage of the actual device. Depending on the input voltages at nodes A and B, the voltage across the load resistor, $R_L$, determines the output state of the device. For example, if both voltages at nodes A and B are high, then both input diodes are conducting and the voltage across resistor $R_i$ is high, otherwise, the voltage across $R_i$ is low. The voltage drop across $R_i$ is transferred to the voltage-controlled voltage source at the delay stage, where the output state is determined.
5.3.2 Linear Resistors

The resistor of the macromodel's input stage, $R_i$, is nonlinear, correctly modeling the input characteristics of the device. However, the resistors of the macromodel's output stage, $R_{ad}$ and $R_{ah}$, are linear. The output stage resistors provide an approximation to the nonlinear output resistance of the actual device. The linear resistors simplify the macromodel and deter convergence problems during simulation. It is possible to substitute nonlinear resistors for the linear resistors, but convergence problems are almost certain to occur.

Referring to Figure 5.2.1, the output resistors, $R_{ad}$ and $R_{ah}$, are functions of the voltage across the resistors, $V_{R_{ad}}$ and $V_{R_{ah}}$, and the current flowing through the resistors, $I_{ad}$ and $I_{ah}$, respectively. If nonlinear output resistors are desired, the resistors can be defined in terms of nonlinear functions of voltage and current. The procedure
for creating a look-up table of nonlinear output resistors is as follows:

1) set up a circuit simulation to measure the output I-V data with the device in the low state,

2) determine the output current from the actual device in the low state, \( I_o \),

3) determine the voltage across the macromodels output low resistor \( R_{cl} \), \( V_{R_{cl}} \), by subtracting \( V_o \) from \( V_{o} \),

4) create a voltage-current table of \( V_{R_{cl}} \) versus \( I_{cl} \),

5) repeat steps 1-4 for the output high state.

The nonlinear output resistors are implemented in PSpice with a voltage-controlled current source in the form of a look-up table. The nonlinear resistors provide improved accuracy of the output characteristics, but convergence is not assured.

5.3.3 Linear Capacitors

All capacitors of the macromodel are linear. The linear capacitors provide an approximation to the nonlinear capacitance of the input and output stages. Since the input capacitance of the device does not vary much as a function of the input voltage, the linear input capacitor of the macromodel provides a good approximation to the nonlinear input capacitance of the device. In addition, the output capacitance is a function of the state of the device. When the output is in the low and high states, the output capacitance is modeled by \( C_{cl} \) and \( C_{ch} \), respectively. Hence, the effective out-
put capacitance is nonlinear, consisting of two linear capacitors which are functions of the output state.

PSpice does not provide a nonlinear capacitor model. However, other analog circuit simulators exist which provide nonlinear capacitor models in the form of look-up tables or polynomials. The nonlinear capacitor is often defined in terms of charge and voltage, since charge distribution provides a better model of the physical process. If better accuracy is required, the macromodel must be modified to run in an analog circuit simulator which supports a nonlinear capacitance model.

5.3.4 Convergence Problems

Convergence problems occur due to an inability to achieve a DC or transient bias point solution. Two causes of convergence problems can occur with the macromodel: the configuration of components in the circuit, and the look-up table or polynomial definition.

The configuration of the model components in the circuit can cause convergence problems. The macromodel is an awkward circuit for an analog circuit simulator. The macromodel consists of nonlinear voltage-controlled voltage sources and nonlinear voltage-controlled current sources which are dependent on other voltages in the circuit. The short transmission line used as a delay model causes long run times which contributes to convergence problems. The nonlinear switches at the output stage are voltage dependent, contain large resistors, and provide gain when switching, which also causes convergence problems. In addition, the ground noise inductors can cause
convergence problems during transient analysis, particularly for large rise times. Care must be taken to ensure that the circuit is constructed carefully, avoiding any circuit loops which may cause convergence problems.

The look-up tables of nonlinear voltage-controlled voltage sources and nonlinear voltage-controlled current sources are possible causes of convergence problems. The tables must be defined for all possible voltages incurred during simulation. If a dependent node voltage does not correspond to a voltage in the table, then convergence problems can occur. Undefined dependent voltage values not in the table are extrapolated from the other voltage values in the table, and produce unpredictable and unwanted results which cause convergence problems. This holds true for voltage-controlled sources defined by polynomials as well. Undefined dependent voltages calculated by the polynomial produce large extrapolated values and often unpredictable results.

5.4 Conclusion

This chapter presented a 74F00 NAND gate macromodel. The macromodel was constructed based on the one-port and two-port techniques presented in Chapters 3 and 4. The macromodel consisted of an input stage, a delay stage, and an output stage. The input stage modeled the input characteristics of the device. The delay stage modeled the propagation delay of the device. The output stage modeled the output characteristics and logic operation of the device. The macromodel was implemented in PSpice, a commercial analog circuit simulator.
Scattering parameter results for the one-port macromodels were presented. For the input stage, the magnitude and phase of the measured $S_{11}$ and the optimized $S_{11}$, as a function of input bias voltage and frequency were presented. For the output stage, the magnitude and phase of the measured $S_{22}$ and the optimized $S_{22}$ as a function of the output state of the device and frequency were presented. In addition, tables of the optimized model components were presented. Good agreement was obtained.

Problems and limitations of the macromodel were presented. The problems and limitations of the macromodel included: the single-input stage, the linear output resistors, the linear input and output capacitors, and convergence problems. If additional accuracy or functionality is required, the macromodel can be modified to correct the problems and limitations. However, a different analog circuit simulator may be needed, and convergence is not guaranteed.

Chapter 6 presents DC and transient results of the 74F00 macromodel. The results include comparisons between the macromodel and the transistor-level model.
Chapter 6
Results and Discussion

6.1 Introduction

This chapter presents DC and transient analysis results which verify the operation of the 74F00 NAND gate macromodel. A DC analysis was performed on the input and output stages of the macromodel. The DC analysis included the input and output I-V curves and the voltage transfer characteristics of the macromodel. In addition, a transient analysis was performed on two macromodel circuits. The DC and transient analysis results were compared to those of the transistor-level model.

Three DC analyses were performed on the macromodel. The first analysis consisted of the input I-V curve of the macromodel. The second analysis consisted of the output I-V curves of the macromodel. Two output I-V curves are presented: the device in the low state and the device in the high state. The third analysis consisted of the voltage transfer characteristics of the macromodel. The voltage transfer characteristics described the output voltage as a function of the input voltage.

Two transient analyses were performed on the macromodel. The first analysis was on a simple circuit, consisting of a NAND gate terminated in a resistive and capacitive load. The second analysis involved a more complex circuit, a NAND gate driver and receiver network commonly found in digital circuit design. The circuit consisted of two NAND gates separated by a transmission line with the second gate terminated in a resistive and capacitive load.
6.2 Results of DC Analysis

The purpose of this section is to verify the DC characteristics of the 74F00 NAND macromodel. DC analyses were performed on the macromodel using PSpice which included the input I-V curve, the output I-V curves, and the voltage transfer characteristics. The DC analysis results of the macromodel were compared to those of the transistor-level model.

6.2.1 Input I-V Curve

The input I-V curve of the macromodel was obtained from a SPICE simulation. The circuit configuration consisted of the macromodel with a sweeping DC voltage source and an ammeter at the input and a 10 kΩ load at the output. The DC voltage source at the input was swept from 0.0 to 6.0 volts, and the corresponding input current was measured. The circuit configuration for measuring the input I-V curves is shown in Figure 6.2.1. A comparison of the macromodel's input I-V curve to the transistor-level model's input I-V curve is shown in Figure 6.2.2. The agreement was excellent.
6.2.2 Output I-V Curves

The output I-V curves of the macromodel were obtained from a SPICE simulation. Two output I-V curves are presented: the output in the low state, and the output in the high state. The circuit configuration consisted of the macromodel with both a sweeping DC voltage source and an ammeter at the output. In addition, a fixed voltage source at the input was included to control the state of the output. The DC voltage source at the output was swept from 0.0 to 6.0 volts, and the corresponding output current was measured. The circuit configuration for measuring the output I-V curves is shown in Figure 6.2.3. A comparison of the macromodel's output low and output high I-V curves to the transistor-level model's output low and output high I-V curves is shown in Figures 6.2.4 and 6.2.5, respectively.

Recall that the output resistors were linear, thus the output I-V curves were linear approximations to the actual device's nonlinear output I-V curves. The output low I-V curves agreed well up to 0.3 volts. From 0.3 to 5.0 volts, the macromodel's I-V curve did not follow the nonlinearity of the transistor-level model's I-V curve. The output high I-V curves agreed well from 0.0 to 3.3 volts. From 3.3 to 5.0 volts, the macromodel's I-V curve provided a linear approximation only and did not follow the nonlinearity of the transistor-level model's I-V curve.
Figure 6.2.2: Comparison of input I-V curve of the macromodel (---) and the transistor-level model (-----) for the FAST TTL NAND gate.
Figure 6.2.3: Circuit configuration for simulating the output I-V curve

6.2.3 Voltage Transfer Characteristics

The voltage transfer characteristics of the macromodel were obtained from a SPICE simulation. The circuit configuration consisted of a sweeping DC voltage source at the input and a 1 kΩ load at the output. The 1 kΩ load was arbitrary, however, the voltage transfer characteristics were a function of the output load. The DC voltage source at the input was swept from 0.0 to 5.0 volts, and the corresponding output voltage was measured. A comparison of the macromodel’s voltage transfer characteristics and the transistor-level model’s voltage transfer characteristics is shown in Figure 6.2.6. The agreement was good.

6.3 Results of Transient Analysis

The purpose of this section is to verify the transient behavior of the 74F00 NAND gate macromodel. Two transient analyses were performed using PSpice. The first transient analysis was on a NAND gate terminated in a resistive and capacitive load. The second analysis was on a NAND gate driver-receiver network. The transient
Figure 6.2.4: Comparison of output low I-V curve of the macromodel (---) and the transistor-level model (----) for the FAST TTL NAND gate.
Figure 6.2.5: Comparison of output high I-V curve of the macromodel (---) and the transistor-level model (——) for the FAST TTL NAND gate.
Figure 6.2.6: Comparison of voltage transfer characteristics of the macromodel (---) and the transistor-level model (-----) for the FAST TTL NAND gate.
analysis results of the macromodel were compared to those of the transistor-level model.

6.3.1 Simple NAND Gate Circuit

Two transient analysis simulations were performed on the simple NAND gate circuit: one using the macromodel and one using the transistor-level model. The NAND gate circuit, shown in Figure 6.3.1, consisted of a source resistance and a NAND gate terminated in a resistor and capacitor in shunt. The source resistor, $R_s$, was $100 \ \Omega$. The load resistor, $R_l$, and the load capacitor, $C_l$, were $1 \ \text{k\,\Omega}$ and $20 \ \text{pF}$, respectively. The load resistor and the load capacitor represented a fanout load consisting of four digital devices. The input waveform consisted of a trapezoidal pulse with an amplitude of 5 V, a rise and fall time of 5 ns, a pulse width of 10 ns, and a period of 30 ns. The trapezoidal pulse resembled a clock pulse used in digital circuits. To ensure the accuracy of the results over several waveform periods, a pulse duration of 100 ns was used.

The transient analysis results, comparing the output waveforms of the macro-
model circuit to those of the transistor-level model, are shown in Figure 6.3.2. Good agreement was obtained. There was some ringing in the macromodel waveform due to the large ground inductance of the macromodel and the capacitive loading. In addition, the rise time of the macromodel waveform did not precisely track that of the transistor-level model waveform due to the nonlinear output voltage-controlled voltage sources and the output capacitance of the macromodel.

The macromodel provided a significant computational speed increase over the transistor-level model. The macromodel and transistor-level model circuits were simulated using PSpice on an 80386 20 MHz IBM compatible personal computer. The total simulation time for the transient analysis of the NAND gate macromodel circuit was approximately 1 minute. Whereas, the total simulation time for the transient analysis of the transistor-level model circuit was approximately 9 minutes. Therefore, the macromodel provided a factor of 9 computational speed increase over the transistor-level model.

6.3.2 A NAND Gate Driver-Receiver Circuit

Two transient analysis simulations were performed on the NAND gate driver-receiver circuit: one using the macromodel, and one using the transistor-level model. The driver-receiver circuit, shown in Figure 6.3.3, consisted of a source resistance and a NAND gate driver and NAND gate receiver separated by a transmission line. The driver was terminated in a shunt resistor. The receiver was terminated in a resistor and capacitor in shunt. The source resistor, $R_s$, and the termination resistor, $R_t$,
Figure 6.3.2: Comparison of transient analysis of the macromodel (-- ----) and the transistor-level model (-----) for the simple FAST TTL NAND gate circuit
were 100 Ω. $R_d$ provided parallel termination to minimize ringing in the circuit. The transmission line was a lossless line with a characteristic impedance, $Z_o$, of 50 Ω and a propagation delay, $t_d$, of 10 ns. The load resistor, $R_l$, and the load capacitor, $C_l$, were 10 kΩ and 20 pF, respectively. The input waveform consisted of a trapezoidal pulse with an amplitude of 5 V, a rise and fall time of 5 ns, a pulse width of 10 ns, and a period of 30 ns. The duration of the pulse was 100 ns.

The transient analysis results, comparing the output waveform of the macromodel circuit to that of the transistor-level model, are shown in Figure 6.3.4. Good agreement was obtained. The amplitude of the macromodel waveform was smaller than that of the amplitude of the transistor-level model waveform. This was due to the voltage values used for the voltage-controlled voltage source, $V_{out}$. There was a glitch which occurred at the lowest and highest transitions of the macromodel waveform. This was due to the large ground inductance of the macromodel. In addition, the rise time of the macromodel waveform did not precisely track that of the transistor-level model waveform due to the nonlinear output voltage-controlled voltage sources and the output capacitance of the macromodel.
Figure 6.3.4: Comparison of transient analysis of the macromodel (---) and the transistor-level model (-----) for the FAST TTL NAND gate driver-receiver circuit.
Again, the macromodel and transistor-level model circuits were simulated using
PSpice on a 80386 20 MHz IBM compatible personal computer. The total simulation
time for the transient analysis of the NAND gate macromodel driver-receiver circuit
was 6.8 minutes. Whereas, the total simulation time for the transient analysis of the
transistor-level model circuit was 34.3 minutes. Thus, the macromodel provided a
factor of 5 computational speed increase over that of the transistor-level model. The
speed increase was approximately 55 percent smaller than that of the simple NAND
gate circuit presented previously. This was due to the transmission line present in
the driver-receiver circuit. The transmission line required a small time-step which
resulted in a longer run time, thus reducing the macromodel's speed advantage.

6.4 Conclusion

This chapter presented DC and transient analysis results of the 74F00 NAND gate
macromodel. The DC analysis results included the input I-V curve, the output I-V
curves, and the voltage transfer characteristics of the macromodel. The transient
analysis results included a simple NAND gate circuit and a NAND gate driver-receiver
circuit. All circuit simulations were performed using PSpice.

Good DC analysis results were obtained. The agreement between the input I-V
curves of the macromodel and the transistor-level model was excellent. The input
stage of the macromodel included a nonlinear resistor to correctly model the input I-V
curve of the device. The agreement between the output I-V curves of the macromodel
and the transistor-level model was good. The linear output resistors provided a
good approximation to the nonlinear output resistance of the device. The agreement between the voltage transfer characteristics of the macromodel and the transistor-level model was also good.

In addition, good transient analysis results were obtained. Two transient analyses were performed. First, a transient analysis of a simple NAND gate circuit was performed. The agreement between the macromodel output waveform and the transistor-level model output waveform was good. Second, a transient analysis of a NAND gate driver-receiver circuit was performed. Again, good agreement was obtained. Compared to the transistor-level model, the macromodel provided a factor of 9 speed increase for the simple NAND gate circuit and a factor of 5 speed increase for the NAND gate driver-receiver circuit.
Chapter 7
Conclusion

7.1 Summary

The objective of this thesis was to present a technique for developing macromodels of digital integrated circuits for high-speed digital circuit simulation. The report consisted of three parts: a review of macromodeling theory, a discussion of the techniques for developing one-port and two-port macromodels, and the development and discussion of a TTL NAND gate macromodel.

In the first part of the thesis, a review of macromodeling theory was presented. The review consisted of six common macromodel types, several macromodel examples, and one-port and two-port macromodel definitions. Three macromodel examples were presented. The examples were TTL NAND gates, developed by Bakhov, Greenbaum, and Glesner in the 1970s and early 1980s. The one-port and two-port macromodel definition described the one-port and two-port models, the type of components used, and the measurement techniques used in extracting the model components.

In the second part of the thesis, techniques for developing one-port and two-port macromodels of digital integrated circuits were presented. With the one-port macromodels, the input and output characteristics of TTL devices were presented, including a FAST TTL NAND gate example. The macromodel components were extracted using DC and frequency-domain measurement techniques. The DC measurements consisted of the input and output I-V curves of the device, whereas the frequency-
domain measurements consisted of scattering parameter measurements. The model components were calculated by equating the analytical impedance and admittance equations of the model to the measured impedance and admittance of the device obtained from DC and frequency-domain measurements. A FORTRAN routine was used to calculate the model components as a function of applied bias voltage. Optimization of the model and the actual device was performed using CAD software to further verify the accuracy of the model components' values.

For the two-port macromodel, the complete macromodel, including the internal characteristics of the device, was presented. The internal characteristics consisted of the current drive capability, the logic operation, the propagation delay, and the ground noise modeling of the device.

In the third part of the thesis, the development of a 74F00 NAND gate macromodel was presented. The macromodel was constructed using the one-port and two-port techniques presented in Chapters 3 and 4 and implemented in PSpice, a commercial analog circuit simulator. The three stages of the macromodel, which included an input stage, a delay stage, and an output stage, were discussed. In addition, problems and limitations of the macromodel were discussed.

DC and transient analysis results of the macromodel were presented. The DC analysis results included an input I-V curve, output I-V curves for the device in the low and high states, and a voltage transfer curve. The transient analysis results included a simple NAND gate circuit and a NAND gate driver-receiver circuit. The macromodel results are compared to those of the transistor-level model. Good agree-
ment between the macromodel and the transistor-level model was obtained. The macromodel provided an accurate time-domain model for a FAST TTL NAND gate with a factor of 5 to 10 computational speed increase over that of the transistor-level model.

7.2 Discussion

In the past two decades, macromodeling techniques have become increasingly popular in the CAD community. Macromodels were developed out of a need for a fast model with the accuracy and functionality of the original device. Previous macromodeling techniques were based on two approaches. First, mathematical macromodels were developed which described the device or system by algebraic or differential equations. Second, simplified lumped-element models were developed which were compatible with common analog circuit simulators. However, both approaches lacked the functionality and accuracy of the original device.

The macromodeling technique presented in this thesis offered an improved method for modeling digital integrated circuits using nonlinear table-based models. The macromodel described the input and output characteristics as well as the internal characteristics of the device. Compared to the transistor-level model of the device, the macromodel provided a computationally fast and accurate model. The macromodel can be implemented in an analog circuit simulator for use in high-speed digital circuit simulation.
7.3 Suggestions for Further Study

Due to time constraints, it was not possible to cover all of the topics of this large research area. Additional areas of study include:

1) use of nonlinear output resistors in the output stage of the macromodel,

2) construction of a dual-input model for the NAND gate,

3) improvement of convergence properties of the macromodel,

4) optimization of the macromodel components using the simulated scattering parameters of the transistor-level model of the device,

5) development of macromodels for other digital integrated circuits, including buffers, inverters, flip-flops, and comparators, and additional device technologies, such as CMOS, ACL, ASTTL, ALSTTL, LSTTL, ECL, and GaAs, and

6) implementation of macromodels into TRANSIM [20], an analog circuit simulator for use in high-speed digital circuit simulation.
References


[18] PSpice, MicroSim, Corporation, Irvine, CA.


[20] M. Steer, M. Basel, and J. Hall, TRANSIM, NC State University, Department of Electrical and Computer Engineering.


Related References Not Cited in Paper


Appendix A

Ground Noise in High-Speed Digital Systems

As clock speeds increase in digital systems, circuit parasitics become an important consideration. In particular, the lead inductances due to circuit trace lengths are no longer negligible. With digital systems constructed on printed circuit boards, the lead inductances are due to the finite trace lengths of power and ground plane interconnections and the bond wires of the logic chip packaging.

With small-signal analog circuits, the noise source is due to external noise coupled into the circuit. In contrast, digital circuits operate at large signal levels, and the noise source is primarily internal. Digital circuit noise results from both power supply transients and signal return currents. Power supply transients can be controlled with decoupling capacitors, but signal return currents cannot be decoupled. Transient currents on the ground return path due to transistors switching states is the primary concern. The transient currents cause significant voltage drops in the ground path due to the trace inductance. Therefore, to reduce these voltage drops in the ground path, the inductance of the path, and thus the trace length, must be reduced.

The finite trace length of the ground plane-to-device interconnection is an element which cannot be eliminated in printed circuit board design. Hence, the inductance associated with this length must be a design consideration. However, the inductance due to the bond wire of the device packaging can be reduced by shortening the bond wire lengths. One method of reducing the lead inductance is to move the $V_{cc}$ and
ground pins of the device to the center of the device package.

To illustrate the effect of ground noise, consider the circuit of Figure A.1.1a [21]. Let \( I_g \) represent a transient current shown in Figure A.1.1b. The voltage \( V_g \) is given by

\[
V_g = L_g \frac{dI_g}{dt} = L_g \frac{I_m}{T/2}
\]  \hfill (A.1)

where \( I_m \) is the maximum amplitude of the transient current pulse, \( T \) is the period of the pulse, and \( L_g \) is the ground inductance. The charge across the capacitor is given by

\[
Q = C_i V_i = I_m \frac{T}{2}
\]  \hfill (A.2)
where \( C_l \) is the load capacitance and \( V_l \) is the load voltage. Substituting (A.2) into (A.1) gives
\[
V_s = \frac{4C_lV_lL_g}{T^2}
\]
(A.3)

Applying some typical numerical values for a digital device gives,
\[
V_s = \frac{4(50pF)(3.5V)(10nH)}{(2ns)^2} = 1.8V
\]
(A.4)

Therefore, we have a 1.8 volt ground reference which may cause unwanted switching of other devices in the circuit. This is unacceptable if the digital system is to operate correctly. Other effects of ground noise on system performance include [21]:

1) ground noise is inherent with FAST TTL devices since inputs are referenced to ground,

2) either low or high input voltages will allow the noise margin to be exceeded,

3) the input may switch erroneously,

4) combinatorial logic will slow down or glitch,

5) latches and flip-flops may be clocked inadvertently and stored data may be lost,

6) complex circuits may oscillate,

7) difficulty in measuring input thresholds,

8) at the output, a change in the voltage available will force the discharge current through the pull-down device,

9) substantial undershoot could occur,
10) multiple switching can speed up or slow down the device, and

11) both rise and fall times can be altered by driving pull-up or pull-down stages incorrectly.

Consider a digital circuit with a totem pole output stage, shown in Figure A.1.2 [22]. When the output is in the low state, transistor $Q_1$ is on and transistor $Q_2$ is off. Conversely, when the output is in the high state, transistor $Q_1$ is off and $Q_2$ is on. Both the output low and output high state have a high impedance path between the power supply and ground. However, when the output is switching states, both transistors $Q_1$ and $Q_2$ are on, and a low impedance path from the power supply to ground exists. The low impedance path produces a transient current spike and charges the output capacitor. The transient current spike flows through the power supply inductance and causes a significant voltage drop in the power supply. In addition, the transient
current spike flows through the ground inductance and raises the ground potential.

The power supply voltage drop due to the transient current and the power supply inductance can be eliminated by placing a decoupling capacitor near the digital gate. The decoupling capacitor provides a source of charge and supplies the transient current without drawing it through the power supply and ground inductance. The ground inductance cannot be bypassed by a decoupling capacitor, and must be a consideration in the digital logic design.

To minimize the internal noise caused by the power supply and ground inductance, digital logic systems must be designed with [22]:

1) a low inductance ground system, and

2) a source of charge near each logic gate (decoupling capacitor).
Appendix B

Nonlinear Device Theory with Applications in SPICE

B.1 Nonlinear Capacitors

A nonlinear capacitor can be defined as the derivative of charge with respect to the derivative of voltage, shown in (B.1).

\[ C(v) = \frac{dq}{dv} \]  \hspace{1cm} (B.1)

Rearranging (B.1) and solving for the derivative of charge, \( dq \), gives,

\[ dq = C(v)dv \]  \hspace{1cm} (B.2)

Integrating both sides of (B.2) gives,

\[ q(v) = \int C(v)dv + Q_0 \]  \hspace{1cm} (B.3)

Equation (B.3) gives the charge as a function of voltage and the initial charge, \( Q_0 \).

To model the nonlinear capacitance or nonlinear charge in an analog circuit simulator, one can use a polynomial or a look-up table of capacitance or charge as a function of voltage. In SPICE, a polynomial describes the capacitance as a function of voltage. While in CAzM, an analog circuit simulator with emphasis on macromodeling, look-up tables describe the charge as a function of voltage [23].

The polynomial, which describes the capacitance or charge as a function of voltage, can be created using a polynomial least squares fitting algorithm. The polynomial
has the general form,

\[ C(v) = a_0 + a_1 V + a_2 V^2 + \ldots + a_n V^n \]  \hspace{1cm} (B.4)

\(a_0, a_1, a_2, \ldots\) are the coefficients of the polynomial returned by the least squares fitting algorithm. The units of the coefficients, \(a_n\), are \(F/V^n\), where \(F\) is Farads and \(V\) is volts. A disadvantage with the polynomial model is that not all data can be represented by a polynomial. Often, a more complex function must be used to describe the data.

A look-up table can be used to describe the capacitance or charge as a function of voltage. The look-up table consists of a listing of the capacitance or charge data versus voltage. The look-up table is simple and easy to implement. The measured or simulated data is inserted directly into the circuit simulator. The only restriction with the data is that it be monotonic, either increasing or decreasing, but not both. This restriction ensures minimal convergence problems.

### B.2 Nonlinear Resistors

A nonlinear resistor can be defined as the derivative of voltage with respect to the derivative of current, shown in (B.5).

\[ R(v) = \frac{dv}{di} \]  \hspace{1cm} (B.5)

From (B.5), the nonlinear resistance is simply the slope of the I-V curves of the device.

A polynomial or look-up table can be used to model the nonlinear resistance in analog circuit simulator, such as SPICE. A voltage-controlled current source is used
as a nonlinear resistor, with a polynomial or look-up table describing the current as a function of voltage. The Berkeley version 2G of SPICE supports only polynomials, while PSpice supports both polynomials and look-up tables.

The polynomial, which describes the current as a function of voltage, can be created using a polynomial least squares fitting algorithm. The polynomial has the general form,

$$I(V) = a_0 + a_1 V + a_2 V^2 + \ldots + a_n V^n \quad (B.6)$$

$a_0$, $a_1$, $a_2$, ... are the coefficients of the polynomial returned by the least squares fitting algorithm. The units of the coefficients, $a_n$, are $A/V^n$, where $A$ is amperes and $V$ is volts, or $S/V^{n-1}$, where $S$ is siemens. Thus, the coefficients of the polynomial are used with a voltage-controlled current source to model a nonlinear resistor. The polynomial does not always accurately model the I-V curves of the device, and often a more complex function is needed to model the I-V curves.

If a nonlinear resistor is a function of two or more voltages in the circuit, a multi-dimensional polynomial can be used to model the resistor. The multi-dimensional polynomial consists of a power series of two or more dependent variables. The general form of the power series describing the current, $i$, as a function of $d$ dependent voltages is given by (B.7),

$$i(V_1, V_2, \ldots, V_d) = \sum_{n=0}^{d} c_n \left[ \sum_{m=1}^{d} V_m \right]^n \quad (B.7)$$

Consider an example of a multi-dimensional polynomial describing the current, $i$, as a function of two dependent variables, $V_1$ and $V_2$. The current is given by (B.8),

$$i(V_1, V_2) = \sum_{n=0}^{2} c_n (V_1 + V_2)^n \quad (B.8)$$
Expanding the right hand side of (B.8) and collecting terms gives,

\[ i(V_1, V_2) = c_0 + c_1 V_1 + c_2 V_2 + c_3 V_1^2 + c_4 V_2^2 + c_5 V_1 V_2 \]  \hspace{1cm} (B.9)

Thus, we have a two-dimensional polynomial expression for the current \( i \) in terms of the two node voltages \( V_1 \) and \( V_2 \). The coefficients \( c_0, c_1, c_2, \ldots \) can be used along with a voltage-controlled current source in SPICE to model a nonlinear resistor.

A look-up table can also be used to model the nonlinear resistor. The look-up table has the advantage of being simple to implement and is more accurate than the polynomial. In PSpice, a look-up table of current and voltage data are used with the voltage-controlled current source to model the nonlinear resistor. An example of a nonlinear resistor used in PSpice is shown in Appendix C.
Appendix C

SPICE Circuit File and User’s Guide for the 74F00 NAND Gate Macromodel

The SPICE circuit file for the 74F00 NAND gate macromodel is presented in section C.1. The users' guide for the SPICE circuit file is presented in section C.2.

C.1 SPICE Circuit File for the 74F00 NAND Gate Macromodel

The NAND gate macromodel is implemented in PSpice, version 4.01. PSpice allows analog behavioral modeling with look-up tables and equation defined dependent sources. The PSpice macromodel circuit is not entirely compatible with the standard Berkeley SPICE version 2G. However, the incompatible components can be modified to SPICE version 2G equivalents, presented in section C.2.

*  
*** BEGIN MACROMODEL SUBCIRCUIT ***  
*  
.subckt nand (1,12)  
*  
*** INPUT STAGE ***  
*  
Rsi (1,2) 15  
Lsi (2,3) 3nH  
Gin (20,3) table {v(3,20)} =  
  + -1.00  0.1104000000  
  + -0.90  0.0836000000  
  + -0.80  0.0575700000  
  + -0.70  0.0329400000  
  + -0.60  0.0118900000  
  + -0.50  0.0014440000
+ -0.40 0.0004875000
+ -0.30 0.0004535000
+ -0.20 0.0004430000
+ -0.10 0.0004330000
+ 0.00 0.0004231000
+ 0.10 0.0004131000
+ 0.20 0.0004031000
+ 0.30 0.0003931000
+ 0.40 0.0003830000
+ 0.50 0.0003730000
+ 0.60 0.0003630000
+ 0.70 0.0003530000
+ 0.80 0.0003430000
+ 0.90 0.0003330000
+ 1.00 0.0003229000
+ 1.10 0.0003129000
+ 1.20 0.0003029000
+ 1.30 0.0002929000
+ 1.40 0.0002828000
+ 1.50 0.0002728000
+ 1.60 0.0002627000
+ 1.70 0.0002524000
+ 1.80 0.0000177200
+ 1.90 0.0000043000
+ 2.00 0.0000000100
+ 2.10 0.00
+ 2.20 0.00
+ 2.40 0.00
+ 2.60 0.00
+ 2.80 0.00
+ 3.00 0.00
+ 4.00 0.00
+ 5.00 0.00
+ 6.00 0.00
Cin (3,20) 5pF
*
*** DELAY STAGE ***
*
Ed (4,20) (3,20) 1.0
Td (4,20,5,20) Zo=50 td=2ns
Rd (5,20) 50
*
*** OUTPUT STAGE ***
*
Eoh (6,20) table { v(5,20) } = 
+ -1.00  0.17700 
+ -0.80  0.17700 
+ -0.60  0.17700 
+ -0.40  0.17700 
+ -0.20  0.17700 
+  0.00  0.17700 
+  0.20  0.17700 
+  0.40  0.17700 
+  0.60  0.17700 
+  0.80  0.17700 
+  1.00  0.17730 
+  1.10  0.66750 
+  1.20  0.66750 
+  1.30  2.23100 
+  1.40  3.19200 
+  1.50  3.48300 
+  1.60  3.59500 
+  1.70  3.79000 
+  1.80  3.85900 
+  1.90  3.87000 
+  2.00  3.87200 
+  3.00  3.87200 
+  4.00  3.87200 
+  5.00  3.87200 
+  6.00  3.87200 

Roh (6,7) 10k
Coh (7,20) 10pF
Soh (7,8) (5,20) slow

* 

Eol (10,20) table { v(5,20) } = 
+ -1.00  3.87200 
+ -0.80  3.87200 
+ -0.60  3.87200 
+ -0.40  3.87200 
+ -0.20  3.87200 
+  0.00  3.87200 
+  0.20  3.87200 
+  0.40  3.87200 
+  0.60  3.87200 
+  0.80  3.87200 
+  1.00  3.87000 
+  1.10  3.85900 
+  1.20  3.79000
+ 1.30  3.59500
+ 1.40  3.48300
+ 1.50  3.19200
+ 1.60  2.23100
+ 1.70  0.66750
+ 1.80  0.17730
+ 1.90  0.17700
+ 2.00  0.17700
+ 3.00  0.17700
+ 4.00  0.17700
+ 5.00  0.17700
+ 6.00  0.17700

Rol (10,9) 20
Col (9,20) 5pF
Sol (9,8) (5,20) shigh

* Lo (8,12) 2nH

* Lg (20,0) 10nH

* .ends nand

* *** MODEL DEFINITIONS FOR SWITCHES ***

* .model slow vswitch (von=0.0 voff=2.0 ron=1.0 roff=10k )
  .model shigh vswitch (von=2.0 voff=0.0 ron=1.0 roff=10k )

* *** END OF MACROMODEL SUBCIRCUIT ***

* C.2 User's Guide

The user's guide defines the PSpice circuit syntax and circuit components for the NAND macromodel circuit file presented in section C.1. In addition, all components incompatible with the standard SPICE version 2G are listed along with their SPICE version 2G equivalents.
C.2.1 Linear Discrete Components

The linear resistors, capacitors, and inductors are described using standard SPICE syntax. Refer to a SPICE manual for further explanation [24].

C.2.2 Lossless Transmission Line

The lossless transmission line is a four terminal device. The transmission line is described by its characteristic impedance and its time delay. For the 74F00 NAND macromodel, a characteristic impedance of 50 Ω and a time delay of 2 ns is used. The lossless transmission line is a standard SPICE component. Refer to a SPICE manual for further explanation [24].

C.2.3 Voltage-Controlled Dependent Sources

The dependent sources consist of voltage-controlled voltage sources and voltage-controlled current sources. The voltage-controlled dependent sources can represent linear or nonlinear functions of voltage or current. The linear voltage-controlled dependent sources are described by a gain or transconductance factor. The nonlinear voltage-controlled dependent sources are described by a look-up table or a polynomial.

The general form of a linear voltage-controlled voltage source (VCVS) is

\[ E_{xxxx} (n1,n2) (nd1,nd2) \text{ gain} \]

\[ E_{xxxx} \] is the component's name. \( n1 \) and \( n2 \) are the nodes of the source. \( nd1 \) and \( nd2 \) are the dependent nodes of the source. \text{gain} is the voltage gain of the source.
The general form of a linear voltage-controlled current source (VCCS) is

\[ G_{xxxxx} (n1,n2) (nd1,nd2) transconductance \]

\( G_{xxxxx} \) is the component's name. \( n1 \) and \( n2 \) are the nodes of the source. \( nd1 \) and \( nd2 \) are the dependent nodes of the source. \( transconductance \) is the transconductance, \( g \), of the source, where \( i = g \times v \).

The nonlinear voltage-controlled dependent sources can be described by a look-up table or a polynomial. The polynomial representation is SPICE 2G compatible, while the look-up table representation is unique to PSpice. Both the polynomial and the look-up table syntax is presented.

The general form of a nonlinear voltage-controlled voltage source described by a polynomial is

\[ Exxxxx (n1,n2) poly(n) (nd1,nd2,...) a0 a1 a2... \]

\( poly(n) \) describes the polynomial dimension. The default for \( poly \) is 1. \( nd1, nd2, ... \) are the dependent nodes corresponding to the dimension of the polynomial. For example, if the polynomial is two-dimensional (a function of two voltages in the circuit), then \( poly(2) \) is used with four dependent nodes. \( a0 a1 a2 ... \) are the polynomial coefficients.

The general form of a nonlinear voltage-controlled voltage source described by a look-up table is

\[ Exxxxx (n1,n2) table\{expression\} = \]

The \textit{table} command specifies a look-up table is to be used. \textit{expression} can be any voltages in the circuit. The format for \textit{expression} is \( v(n1,n2) \), where \( n1 \) and \( n2 \) are
the voltage nodes. The look-up table follows the command line with a continuation delimiter in the first column.

The general form of a nonlinear voltage-controlled current source described by a polynomial is

\[ G_{xxxx} (n1, n2) \text{ poly}(n) (nd1, nd2, ...) a0 a1 a2 ... \]

The command line arguments are identical to the nonlinear voltage-controlled voltage source described by a polynomial.

The general form of a nonlinear voltage-controlled current source described by a look-up table is

\[ G_{xxxx} (n1, n2) \text{ table\{expression\} = } \]

The command line arguments are identical to the nonlinear voltage-controlled voltage source described by a look-up table.

C.2.4 Nonlinear Discrete Components

Nonlinear resistors, nonlinear capacitors, and nonlinear inductors can be modeled in SPICE. Version 2G of SPICE models a nonlinear capacitor and nonlinear inductor by using a polynomial. In contrast, PSpice does not provide a model of a nonlinear capacitor and a nonlinear inductor. A nonlinear resistor can be described by a voltage-controlled current source, which is valid in both version 2G of SPICE and PSpice.

The general form of a nonlinear capacitor in version 2G of SPICE is

\[ C_{xxxx} (n1, n2) \text{ poly co c1 c2 ... } \]
n1 and n2 are the positive and negative nodes of the capacitor, respectively. *poly* is a command line argument signifying polynomial coefficients will follow. c0 c1 c2 ... are the polynomial coefficients expressed as a function of voltage across the capacitor.

The general form of a nonlinear inductor in version 2G of SPICE is

\[ L_{xxxx} \ (n1, n2) \ poly \ l0 \ l1 \ l2 \ ... \]

n1 and n2 are the positive and negative nodes of the inductor, respectively. l0 l1 l2 ... are the polynomial coefficients expressed as a function of current through the inductor.

The nonlinear resistor is described by a voltage-controlled current source. In version 2G of SPICE, a polynomial is used to describe the nonlinear resistor. In PSpice, a polynomial or a look-up table may be used to describe the nonlinear resistor. Refer to the Voltage-Controlled Dependent Sources section above for the general form of the voltage-controlled current source. To convert the voltage-controlled current source to a nonlinear resistor, simply equate the source nodes and the dependent nodes. Thus, the current through the device is a function of the voltage across the device, which describes a nonlinear resistor.

### C.2.5 Nonlinear Switches

The nonlinear switches are used as ideal switches to turn on and turn off parts of the output stage. The switches act as voltage-controlled nonlinear resistors. The switches are described by a model statement, which defines the turn-on and turn-off voltages and the corresponding resistance. The voltage-controlled switches are a PSpice component, and version 2G of SPICE does not have an equivalent component.
The general form of the voltage-controlled switch is

\[ S_{xxxxx}(n1,n2)(nd1,nd2) \text{ model} \]

\( n1 \) and \( n2 \) are the positive and negative nodes of the device, respectively. \( nd1 \) and \( nd2 \) are the positive and negative dependent nodes of the device, respectively. \textit{model} is the name of the switch model. The general form of the switch model statement is

\texttt{.MODEL name vswitch(von voff ron roff)}

\texttt{name} is the model name. \texttt{vswitch} is a command line argument specifying a voltage-controlled switch. \texttt{von} and \texttt{voff} are the turn-on and turn-off voltages, respectively. \texttt{ron} and \texttt{roff} are the corresponding turn-on and turn-off resistances, respectively.